CMX7364

Multi Mode High Performance Wireless Data Modem

D/7364_FI-8.x/3 September 2023 **DATASHEET** Provisional Issue

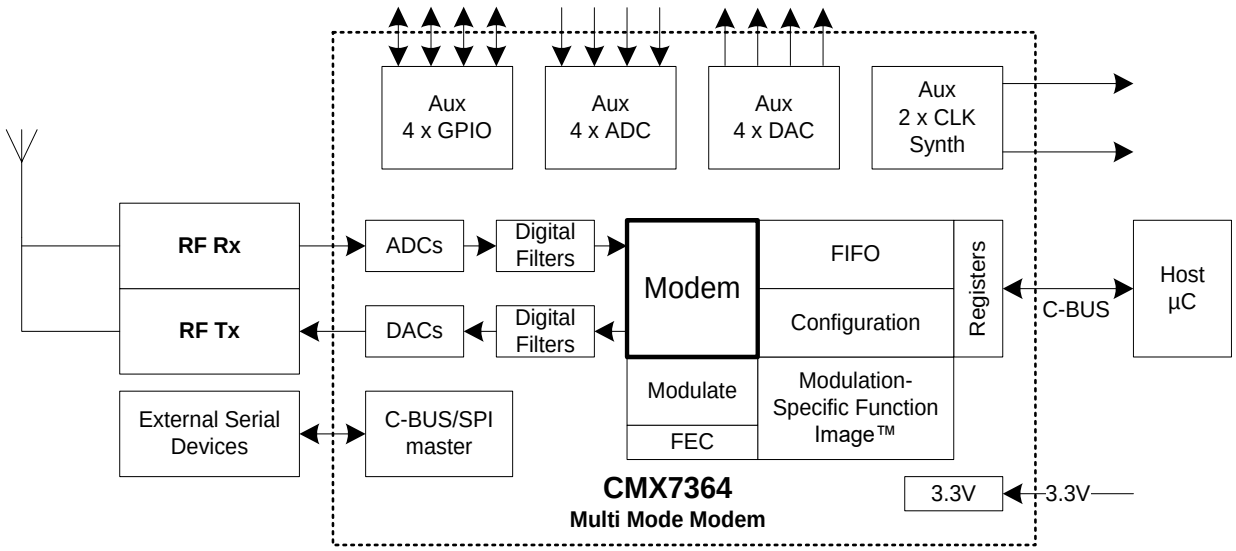
7364FI-8 RTK Modem

Features

- Half-duplex modem for RTK applications
- 7364FI-8.x
  - 4-FSK 4800 and 9600 ksymbols/s for use in 12.5kHz and 25kHz channels
  - Compatible with RTCM SC135
  - Two frame sync detectors
  - Automatic frame sync detect
  - Rx carrier frequency correction
  - Receive signal quality measurement
- C-BUS host Serial Interface
  - SPI-like with register addressing
  - Read/Write 128-byte FIFOs and data buffers streamline transfers and relaxed host service latency
- High Performance I/Q Radio Analogue Interface
  - Tx and Rx: 'direct connect' to zero IF transceiver
  - Simple external RC filters
  - Digital IF filter reconfigures for multiple RF channel spacings (Rx)
  - Deviation control without manual trim (Tx)I/Q trims
- Auxiliary Functions
  - Four 10-bit DACs
  - Autonomous RAMDAC sequencer
  - Automatic support for dc calibration of CMX998
  - Four 10-bit ADCs
  - ADC averaging and trip on high/low 'watch' modes
  - Four GPIO
  - Sequence GPIO on Tx or Rx trigger
  - Start Tx on digital trigger input
- Master C-BUS/SPI Serial Interface
  - For external slave devices e.g. RF transceiver and synthesiser
  - Pass-through mode expands host C-BUS/SPI capacity
- Two Synthesised Clock Generators
- Low Power 3.3V Operation with Powersave Functions
- Small 64-pin VQFN Package

Applications

- High Performance Narrowband Data Radio
  - RTCM SC135 compatible
  - RTK/Telemetry/SCADA/data modems
  - 12.5kHz and 25kHz RF channel spacing
  - Compatible worldwide e.g. ETSI, FCC, ARIB, etc.
  - FCC Part 90 per new spectral efficiency requirements
- Digital Software Defined Radio (SDR)
- High-speed Wireless Data
- Mobile Data over Fading Channels



1 Brief Description

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

The CMX7364 Multi Mode Modem is a half-duplex device currently supporting 4-Level FSK modes in 12.5 or 25kHz channel spacings under host control. Its Function Image™ (FI) is loaded to initialise the device and determine modulation types.

The CMX7364 loaded with 7364FI-8.x supports 4-FSK modulation, root raised cosine filtered with α=0.2 with sinc filtering (optional). The CMX7364 FI-8.x supports zero IF (I/Q) and two-point modulation (Mod1/2) transmit modes, with zero IF receive mode. This Function Image™ is largely based on the CMX7364 FI-2 multi-mode modem, but has been optimised for use solely with RTCM SC135 style channel coding supporting RTK operations.

High-performance digital IF filters may be reconfigured to support multiple channel spacings via host command. This feature may eliminate the need to switch between multiple, discrete IF filters.

An integrated analogue interface supports ‘direct connection’ to zero IF I/Q radio transceivers with few external components; no external codecs are required.

Intelligent auxiliary ADC, DAC and GPIO sub-systems perform valuable functions and minimise host interaction and host I/O resources. Two synthesised system clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

Function Image™**.** The device utilises CML’s proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7364 operates from a 3.3V supply and includes selectable powersaving modes. It is available in a 64-VQFN package.

NOTE: This Datasheet is the first part of a two-part document.

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Information in this datasheet should not be relied upon for final product design. It is recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
3	• First public release	August 2023
2	• Table 6: default clock settings changed • Figure 44: updated graph to reflect improved performance	March 2022
1	First release	February 2022
A	Draft release	December 2021

2 Block Diagrams

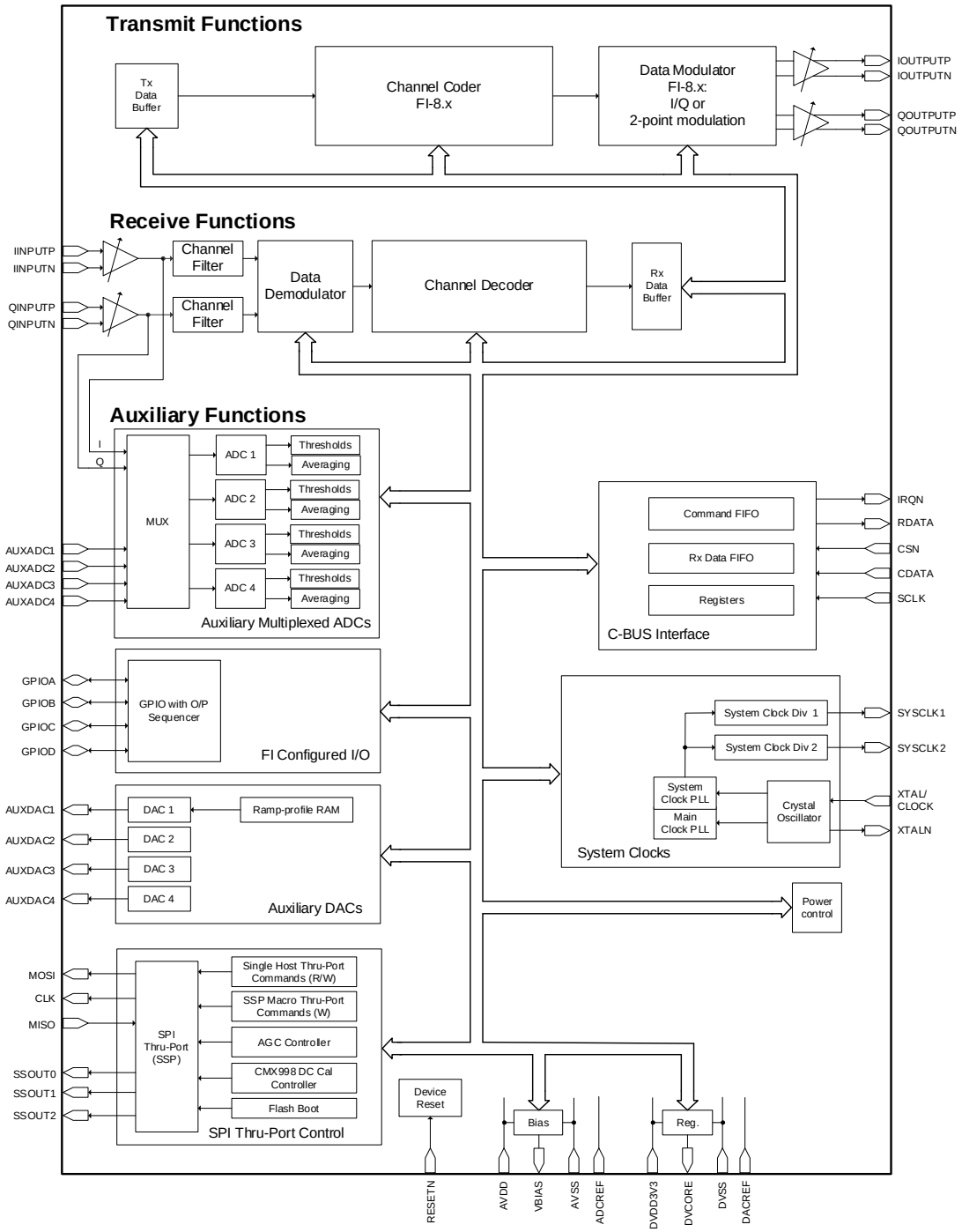


Figure 1 Overall Block Diagram

Figure 1 illustrates the overall functionality of the CMX7364, detailing the auxiliary functions. The following figures expand upon the transmit and receive functions.

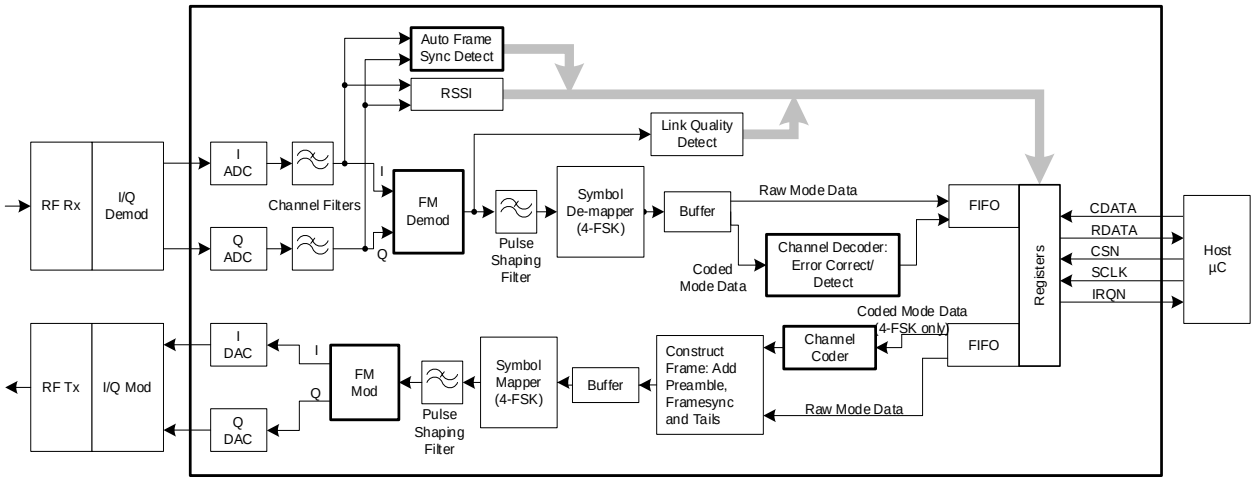


Figure 2 Block Diagram – I/Q Tx and Rx

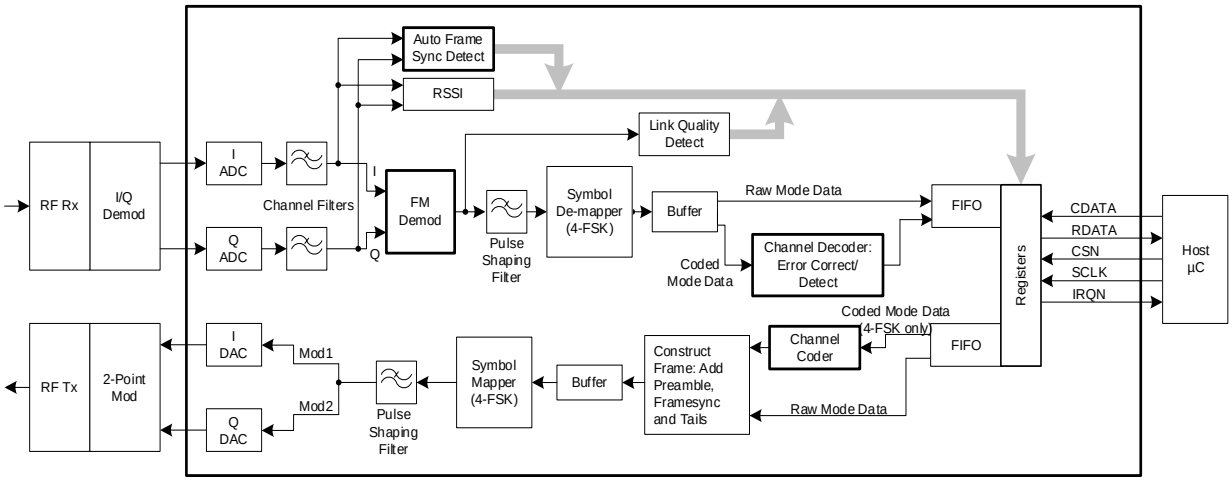


Figure 3 Block Diagram – two-point Tx with I/Q Rx

3 Signal List

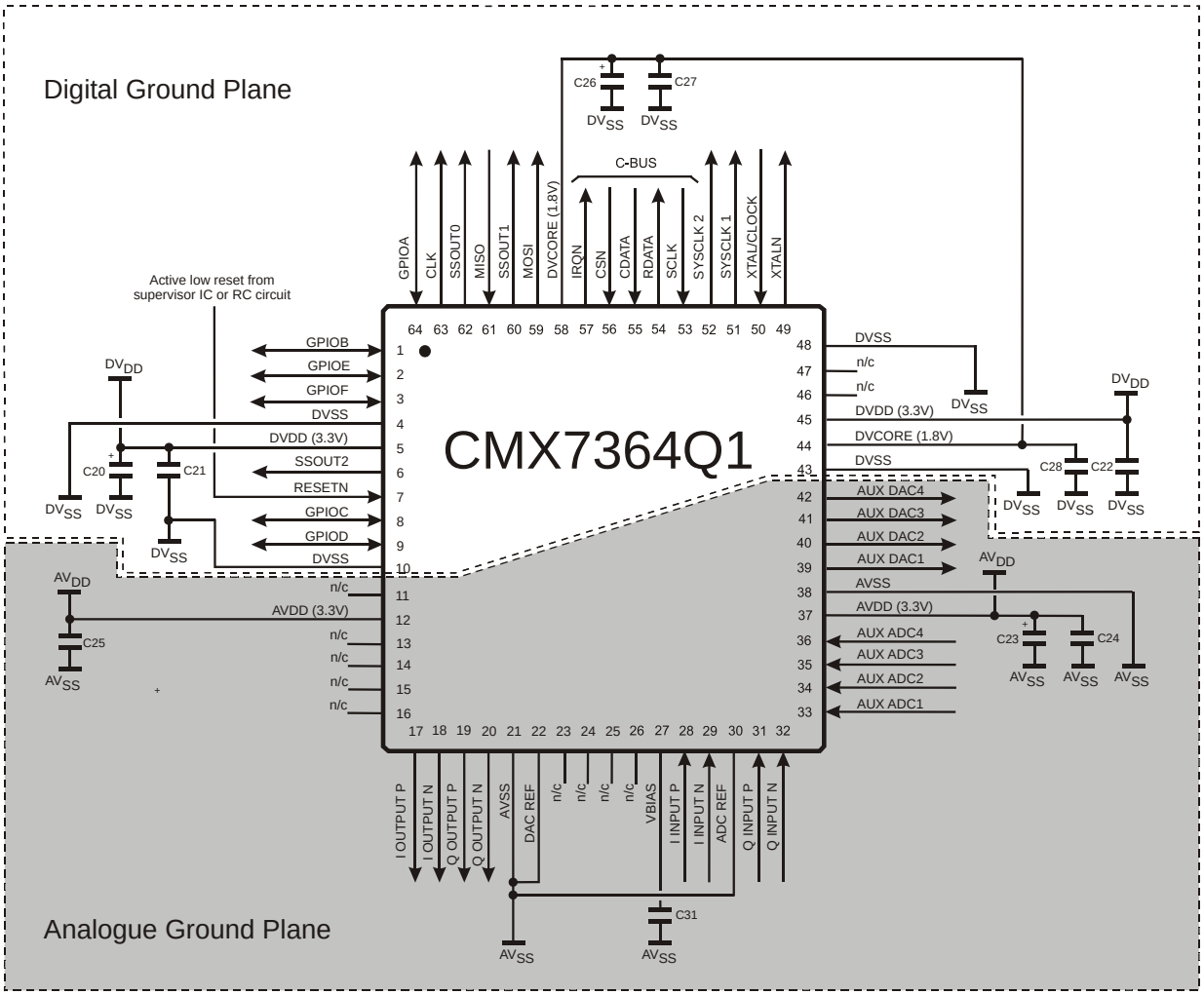
64-pin Q1	Pin		Description
Pin No.	Name	Type	
1	GPIOB	BI	General Purpose I/O
2	GPIOE	BI	General Purpose I/O - reserved
3	GPIOF	BI	General Purpose I/O - reserved
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
5	DVDD 3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	SSOUT2	OP	SPI: Slave Select Out 2
7	RESETN	IP	Logic input used to reset the device (active low)
8	GPIOC	BI	General Purpose I/O
9	GPIOD	BI	General Purpose I/O
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
11	NC	NC	Do not connect
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	NC	NC	May also be connected to AVSS
14	NC	NC	Do not connect
15	NC	NC	Do not connect
16	NC	NC	May also be connected to AVDD
17	IOUTPUTP	OP	Differential outputs for I channel; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the I Output. When in two-point modulation mode the I Output is used as ‘Mod 1’.
18	IOUTPUTN	OP	
19	QOUTPUTP	OP	Differential outputs for Q channel; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the Q Output. When the in two-point modulation mode the Q Output is used as ‘Mod 2’.
20	QOUTPUTN	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF		DAC reference voltage, connect to AVSS
23	NC	NC	Do not connect
24	NC	NC	Do not connect
25	NC	NC	Do not connect
26	NC	NC	Do not connect

64-pin Q1 Pin No.	Pin Name	Pin Type	Description
27	VBIAS	OP	Internally generated bias voltage of approximately $AV_{DD}/2$. If V_{BIAS} is powersaved this pin will be connected via a high impedance to AV_{DD}. This pin must be decoupled to AV_{SS} by a capacitor mounted close to the device pins.
28	IINPUTP	IP	Differential inputs for I channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the I Input.
29	IINPUTN	IP	
30	ADCREF		ADC reference voltage; connect to AV_{SS}
31	QINPUTP	IP	Differential inputs for Q channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the Q Input.
32	QINPUTN	IP	
33	AUXADC1	IP	Auxiliary ADC input 1
34	AUXADC2	IP	Auxiliary ADC input 2
35	AUXADC3	IP	Auxiliary ADC input 3
36	AUXADC4	IP	Auxiliary ADC input 4
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
39	AUXDAC1	OP	Auxiliary DAC output 1 (Optionally the RAMDAC output)
40	AUXDAC2	OP	Auxiliary DAC output 2
41	AUXDAC3	OP	Auxiliary DAC output 3
42	AUXDAC4	OP	Auxiliary DAC output 4
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
44	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DV_{SS} by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect
47	NC	NC	May also be connected to DVSS
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
49	XTALN	OP	Output of the on-chip Xtal oscillator inverter
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source
51	SYSCLK1	OP	Synthesised digital clock output 1
52	SYSCLK2	OP	Synthesised digital clock output 2

64-pin Q1	Pin		Description
Pin No.	Name	Type	
53	SCLK	IP	C-BUS serial clock input from the µC
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC
56	CSN	IP	C-BUS chip select input from the µC
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
59	MOSI	OP	SPI: Master Out Slave In
60	SSOUT1	OP	SPI: Slave Select Out 1
61	MISO	IP	SPI: Master In Slave Out
62	SSOUT0	OP	SPI: Slave Select Out 0
63	CLK	OP	SPI: Serial Clock
64	GPIOA	BI	General Purpose I/O
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad may be electrically unconnected or, alternatively, may be connected to Analogue ground (AVss). **No other electrical connection is permitted.**

Notes:
IP = Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kΩ)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

4 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C31	100nF
C24	10nF		
C25	10nF		

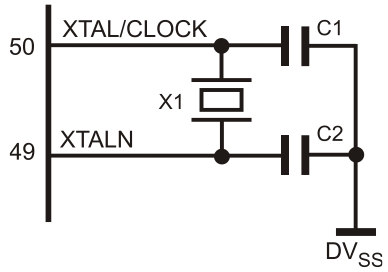
Figure 4 CMX7364 Power Supply and De-coupling

Notes:

To achieve good noise performance, AV_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7364 analogue area to provide a low impedance connection between the AVSS pins and the AV_{DD} and V_{BIAS} decoupling capacitors.

5 External Components

5.1 Xtal Interface



X1 For frequency range see 9.1.2 Operating Limits
C1 22pF Typical
C2 22pF Typical

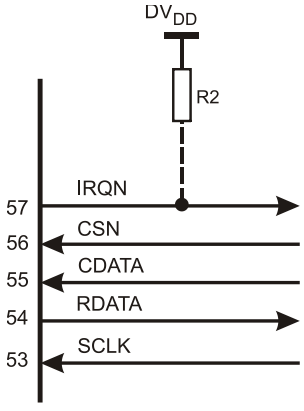
Figure 5 Recommended External Components – Xtal Interface

Notes:
The clock circuit can operate with either a Xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see 9.1.2 Operating Limits. When using an external clock generator the Xtal oscillator circuit may be disabled to save power, see 10.2.3 Program Block 1 – Clock Control for details. Also refer to section 7.1 Xtal Frequency.

The tracks between the Xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane.

The DV_{SS} to the Xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors C1 and C2 refer to the documentation of the Xtal used.

5.2 C-BUS Interface



R2 10k - 100kΩ

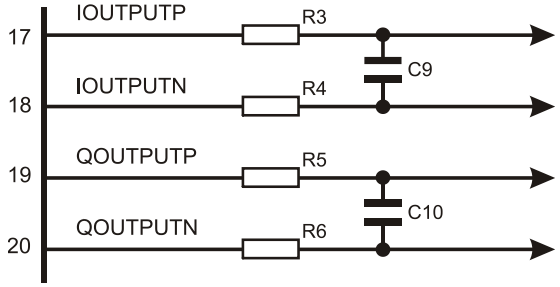
Figure 6 Recommended External Components – C-BUS Interface

Note: If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 I/Q Output Reconstruction Filter

The CMX7364 I/Q Outputs provide internal reconstruction filtering with four selectable bandwidths (-3dB point shown in section 10.1.23). The bandwidth of the internal reconstruction filter may be selected using the I/Q Output Configuration - $B3 write or Signal Control - $61 write registers.

To complete the I/Q output reconstruction filter one of the following external RC networks should be used for each of the differential outputs. The external RC network should have a bandwidth that matches the bandwidth of the selected internal reconstruction filter.



Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
100	22	34
50	20	75
25	22	135
12.5	22	280

Figure 7 Recommended External Components – I/Q Output Reconstruction Filter

When transmitting an I/Q signal, each I/Q output will produce a signal with bandwidth half the channel bandwidth. A reconstruction filter with a –3dB point close to half the channel bandwidth will therefore have significant roll off within the channel bandwidth – which is undesirable. An appropriate choice for channels occupying up to a 25kHz bandwidth (channel bandwidth/2 = 12.5kHz) would be a reconstruction filter of 25kHz bandwidth.

5.4 I/Q Input Antialias Filter

The device has a programmable antialias filter in the I/Q input path, which is controlled using the I/Q Input Configuration - $B0 write or Signal Control - $61 write registers. This should be sufficient for most applications, however if additional filtering is required it can be implemented at the input to the device.

The input impedance of the I/Q Input pins varies with the input gain setting, see section 9.1.3 Operating Characteristics.

5.5 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

If the device is reset (either by asserting RESETN pin 7, issuing a C-BUS General RESET or by triggering an internal power on reset) all GPIO pins will be immediately configured as inputs. Any GPIO pins not being pulled either up or down by an external load will be left in a floating state until the Function Image™ is loaded. To avoid GPIO floating input states that may somewhat elevate supply current between a RESET and Function Image™ load, it will be necessary to connect pull up or pull down resistors of 220kΩ to these pins.

6 General Description

6.1 CMX7364 Features

The CMX7364 is intended for use in half-duplex modems. Transmission takes the form of a data burst consisting of preamble, frame sync and data payload, followed by a tail sequence. Reception may utilise the preamble to assist with signal acquisition[1], but is then followed by frame sync detection and data decoding.

A flexible power control facility allows the device to be placed in its optimum power-save mode when not actively processing signals.

The device includes a Xtal clock generator, with phase locked loop and buffered output, to provide a System Clock output, if required, for other devices.

Block diagrams of the device are shown in section 2, Block Diagrams.

Tx Functions:

- Automatic preamble and frame sync insertion simplifies host control
- I/Q or two-point modulation analogue outputs
- Pulse shape filtering
- RAMDAC capability generates PA power ramping control signal
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching
- Transmit modulation envelope ramping
- Carrier sense for “listen before talk” operation
- Raw data modes
- RTCM SC135 style coded mode

Rx Functions:

- Automatic frame sync detection simplifies host control
- I/Q analogue inputs
- Rx channel filtering and pulse shape filtering
- Channel estimation and equalisation
- Tracking of symbol timing and input I/Q dc offsets
- AGC using SPI Thru-Port
- Raw data modes
- RTCM SC135 style coded mode

Auxiliary Functions:

- Two programmable system clock outputs
- Four auxiliary ADCs with six selectable input paths
- SPI Thru-Port for interfacing to synthesisers, direct conversion receiver (CMX994/A/E), and other external serial interface devices
- Four auxiliary DACs, one with built-in programmable RAMDAC

[1] The frame sync detection algorithm of the CMX7364 is capable of detecting a frame sync without having bit synchronisation, so preamble is not required for obtaining bit sync. Some preamble is still needed to ensure that the beginning of the frame sync is transmitted and received without distortion. Preamble may also be used to provide a known signal on which to acquire I/Q dc offset corrections.

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Four GPIO pins
- Tx trigger input (Provided by GPIOA)
- Serial memory or C-BUS (host) boot mode

6.2 Signal Interfaces (I/Q Tx and Rx)

The transmitted signal is provided as an I/Q baseband, for mixing up onto an RF carrier, with amplification.

In receive, the I/Q interface provides amplitude information, so the RSSI signal is calculated internally. It is averaged in order to produce the RSSI measurement and to support the carrier sense decision whether to transmit.

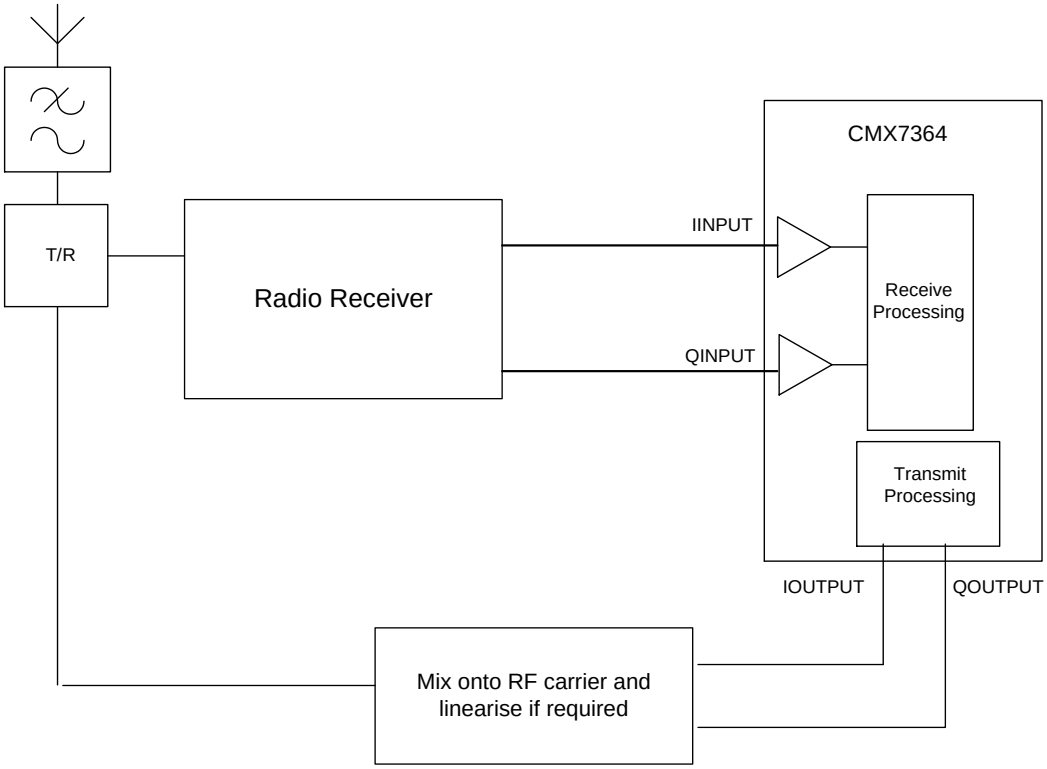


Figure 8 CMX7364 I/Q Tx, I/Q Rx

6.3 Signal Interfaces (Two-point Tx and I/Q Rx)

The device can be configured to produce two-point modulation.

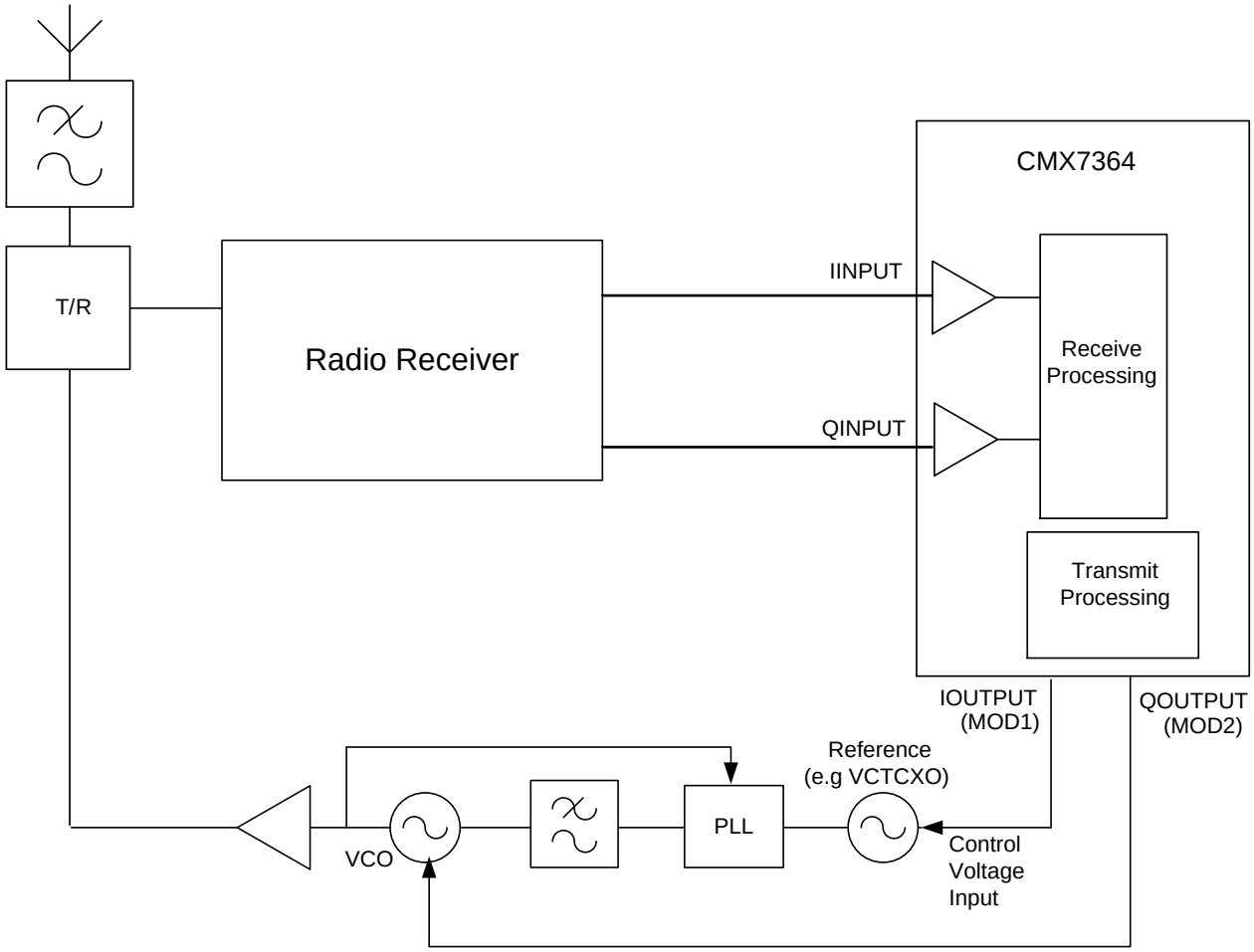


Figure 9 CMX7364 Two-point Tx, I/Q Rx

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7364 is designed to work with a Xtal, or an external frequency oscillator within the ranges specified in section 9.1.3 Operating Characteristics. Program Block 1 (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. Configuration values supporting baud rates up to 40ksymbols/s when the Xtal frequency is 9.6MHz or the external oscillator frequency is 9.6 or 19.2 MHz can be configured. Rates other than those tabulated (within this range) are possible, see section 10.2.3 Program Block 1 – Clock Control, however FI-8 is optimised for use at 4800 and 9600 baud as specified in the RTCM SC135 standard. Further information can be provided on request. The modem can operate with a clock or Xtal input frequency tolerance of 50ppm. The receive performance will be compromised as the system tracks, so a maximum tolerance of 20ppm is recommended.

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7364 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the IRQ Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7364 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single register address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7364's write-only registers, or a data word read out from one of the CMX7364's read-only registers. Streaming C-BUS transactions consist of a single register address byte followed by many data bytes being written to or read from the CMX7364. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 10.

Data sent from the µC on the CDATA (command data) line is clocked into the CMX7364 on the rising edge of the SCLK input. Data sent from the CMX7364 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 9.2 C-BUS Timing gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

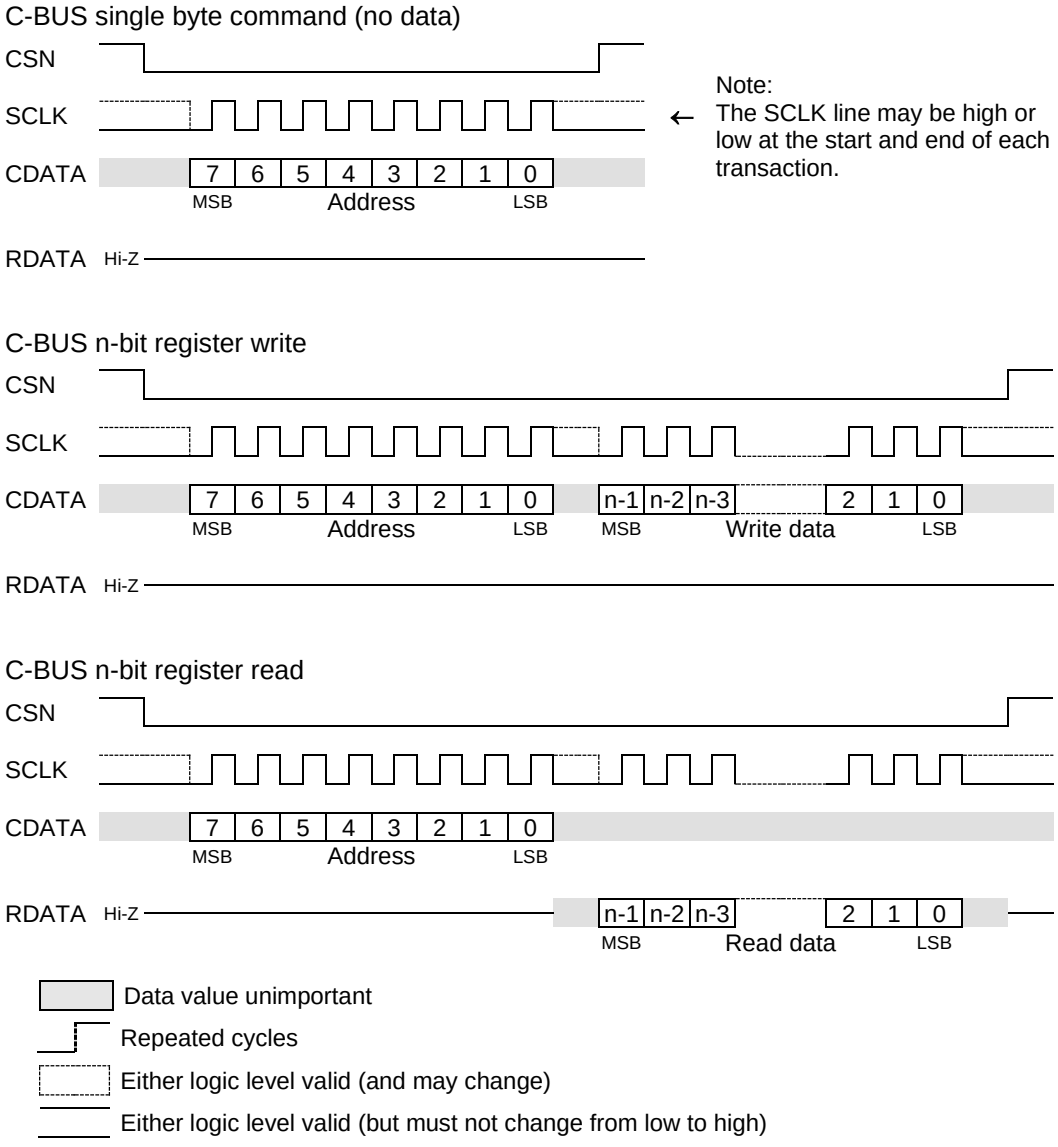


Figure 10 Basic C-BUS Transactions

To increase the data bandwidth between the µC and the CMX7364, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 11.

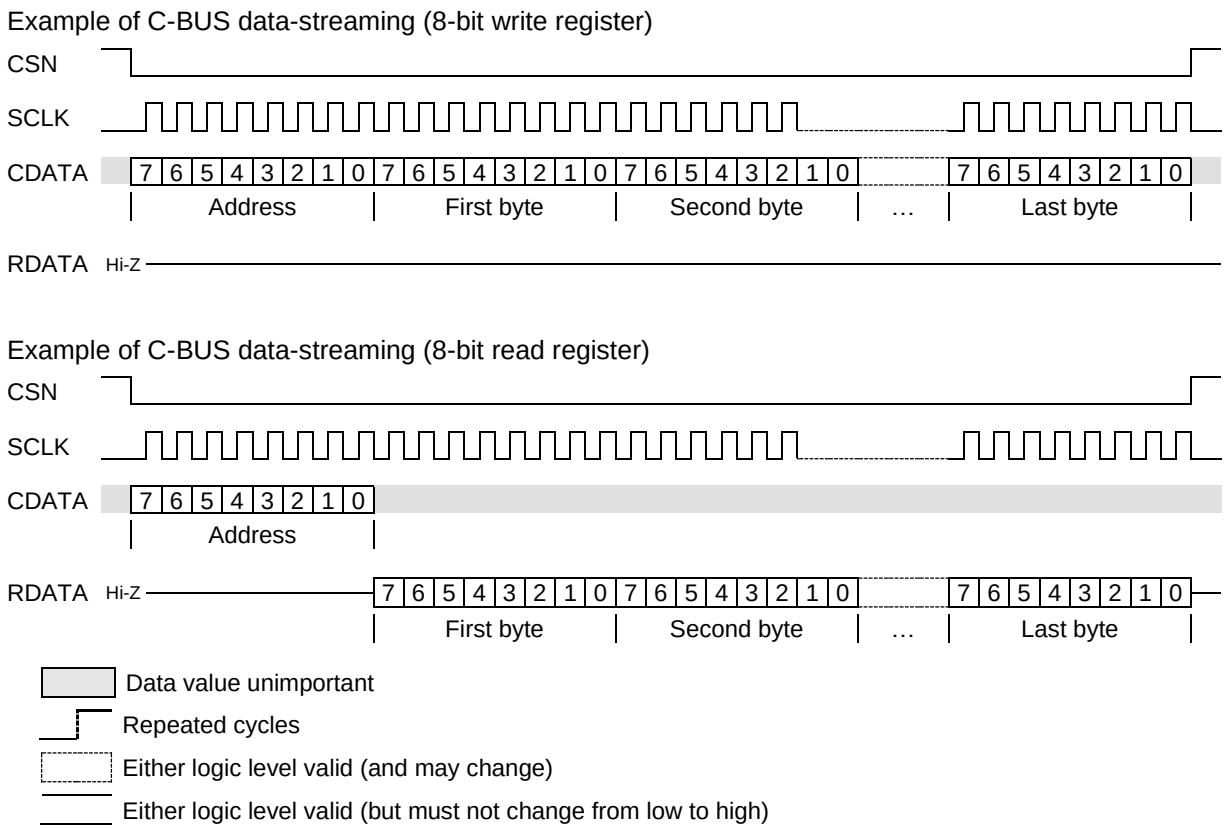


Figure 11 C-BUS Data Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software. The maximum possible size of Function Image™ is 96 kbytes, although a typical FI will be less than this.

The FI can be loaded into the device either by the Host controller via C-BUS, or from a pre-programmed serial memory.

7.3.1 FI Loading from Host Controller

The Function Image™ can be included with the host controller software for download into the CMX7364 at power-up over the C-BUS interface. This is done by writing the FI data into the Tx FIFO Data register, which supports streaming operation.

The device can accommodate the host continuously streaming data to the Tx FIFO at the maximum SCLK rate of 20 MHz; therefore it is not necessary to monitor the FIFO level registers during this operation. FI download time is limited only by the clock frequency of the C-BUS. With a 20 MHz SCLK it should take less than 40ms to complete, even when loading the largest possible Function Image™.

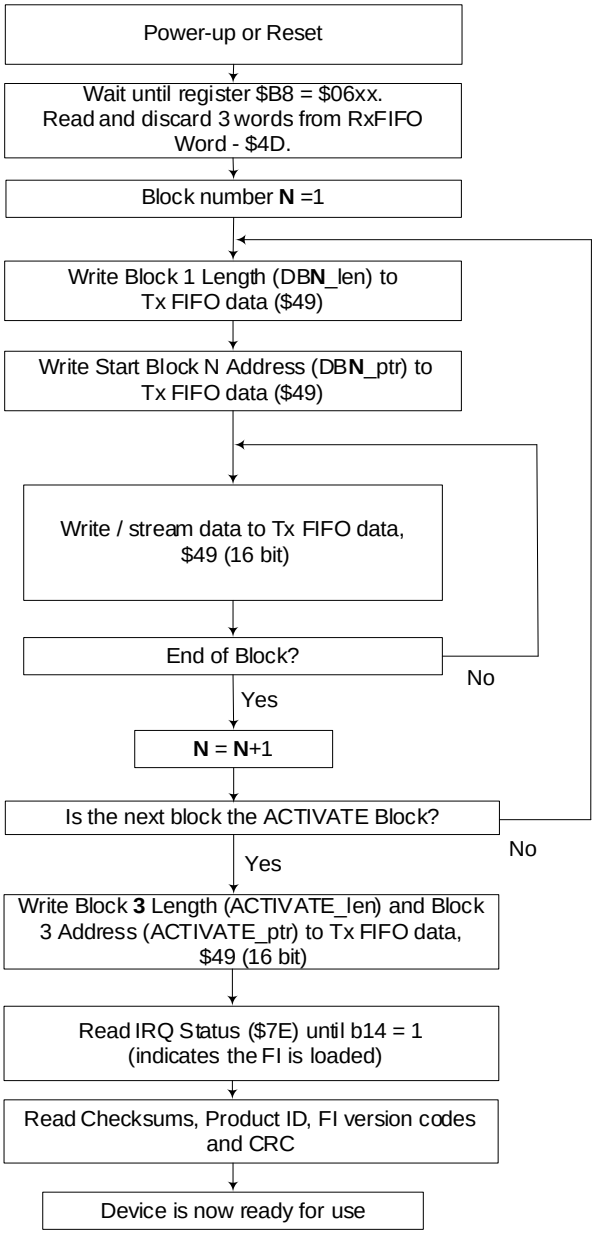


Figure 12 – FI Loading from Host

7.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The serial memory should contain the same data stream as written to the Command (Tx) FIFO shown in **Figure 13**. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7364 SPI Thru-Port using SSOUT0 as the chip select. On power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the host controller must write $0001 to C-BUS register $50. The CMX7364 will then automatically load the data from the serial memory without intervention from the host controller. The default speed for the serial clock is 10MHz. The speed can be changed, if desired, by writing to C-BUS register $52. The speed will then be

40MHz / <$52 register value>. Values of $0000,$0001 and $0002 are reserved, and will result in a speed of 10MHz.

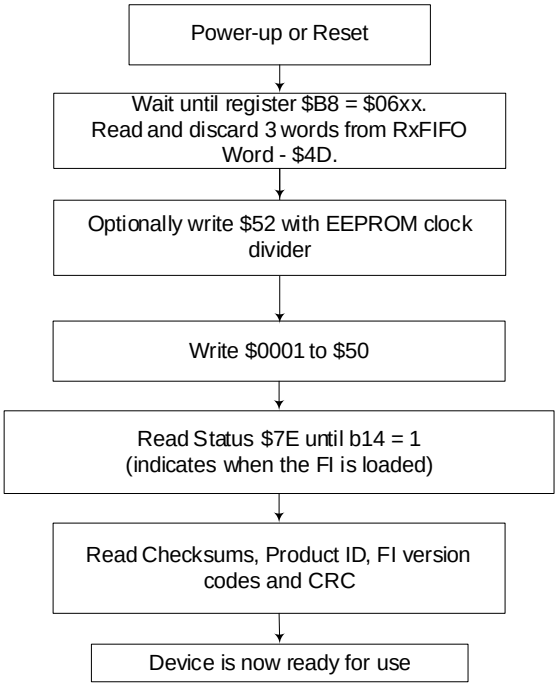


Figure 13 – FI Loading from Serial Memory

The CMX7364 has been designed to function with the Atmel AT25F1024 EEPROM (128K x 8-bits) serial flash device, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 81ms with a 10MHz clock, even when loading the largest possible Function Image™.

7.3.3 Reset without FI Load

Following the RESETN pin becoming high, or following a C-BUS General Reset, the host controller may write $0004 to C-BUS register $50. The CMX7364 will then skip any bootload procedure, and use the previously-loaded FI. In this case, the CMX7364 will not report the 32-bit Block checksums in the Rx FIFO ($4D).

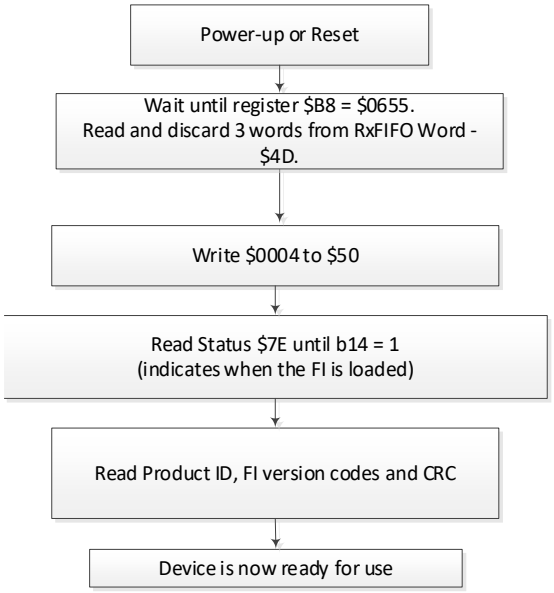


Figure 14 – Reset without FI Load

7.3.4 After FI loading

Once the FI has been loaded, the CMX7364 will report the following information in the Rx FIFO ($4D):

- 32-bit Block 1 Checksum
- 32-bit Block 2 Checksum
- 16-bit Product Ident Code ($7364)
- 16-bit FI version code
- 32-bit FI CRC (generated by the FI).

The host should verify the checksum and CRC values with those published with the Function Image™ file downloaded from the CML Technical Portal.

Once activated, the device initialises fully, enters Tx Off/Rx Off mode and becomes ready for use, and bit 14 of the Status register will be set.

7.4 Device Control

Once the Function Image™ is loaded, the CMX7364 can be set into one of four main modes using the Modem Mode and Control - $6B write register:

- Idle mode – for configuration or low power operation
- Transmit mode – for transmission of raw or formatted data
- Receive mode – for detection and reception of bursts containing raw or formatted data
- Carrier sense mode – for attempting to transmit if the channel is free, otherwise continuing to receive.

These four modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in transmit, receive and carrier sense modes or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in Idle mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power-saving can be achieved by disabling unused hardware blocks, however, most of the hardware power-saving is automatic. Note that V_{BIAS} must be enabled to allow any of the Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- 10.1.18 Programming Register - $6A write
- 10.1.19 Modem Mode and Control - $6B write
- 10.2 Programming Register Operation
- 10.1.25 VBIAS Control - $B7 write.

7.4.1 Normal Operation Overview

In normal operation (after the CMX7364 is configured) the appropriate mode must be selected and data provided in transmit or retrieved in receive. This process is carried out by selecting the mode (Tx, Rx or Carrier Sense), selecting the frame sync to use (Frame Sync 1 or 2) and selecting formatted or raw data. Such a selection is required to initiate transmission or reception of a burst.

In transmit (or following a carrier sense period where no signal is detected on channel) the CMX7364 will begin by switching GPIO signals as configured by the transmit sequence. The RAMDAC can also be configured to ramp up its output signal at this point. Transmission then begins with preamble and the selected frame sync. The main payload of user data comes next, ending with selectable tail bits. The burst ends with the transmission sequence ramping the RAMDAC output signal down and/or switching GPIO signals.

In receive (or following a carrier sense period where signal is detected on channel) the CMX7364 will begin by searching for either or both of the configured frame sync patterns. On detection of a frame sync, reception and delivery of Rx data will begin. Reception continues until the CMX7364 is switched into a different mode, determined by the host.

During the burst, data must be transferred into or out of the CMX7364. Transfers use the Command FIFO to transfer data and commands about data type into the CMX7364, and the Rx FIFO to transfer data out of the CMX7364. The IRQ Status register is used to indicate that the data has been dealt with. The CMX7364 can be configured to interrupt the host when a specified data block has been transferred, or on FIFO fill level.

The CMX7364 offers internal buffering of data in addition to the Command and Rx FIFOs in both receive and transmit directions. The amount of buffering provided depends on the device's operating mode.. In the process of burst transmission or reception the most significant registers are:

- 10.1.19 Modem Mode and Control - $6B write
- 10.1.38 IRQ Status - $7E read
- 10.1.20 IRQ Mask - $6C write
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.27 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.26 Modem Command FIFO Level - $4B read
- 10.1.28 Receive FIFO Level - $4F read

7.4.2 Basic Tx and Rx Operation

The CMX7364 has many features that provide a great deal of flexibility, but basic data transmission and reception can be carried out fairly easily by understanding the operation of just a few registers. There are other ways of controlling signal transmission and reception but basic examples for raw modes are given below:

Basic Transmit Operation

Transmission of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $0080 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous transmissions
Write $18 to the Modem Command FIFO Control Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 8 byte data blocks	Selects blocks of data bytes to be transmitted – 8 bytes in each, after which the CMX7364 will request more data from the host
Write 8 data bytes to the Modem Command FIFO Data Byte - see Modem Command FIFO Data/Control - $48, $49 and $4A write	Pre load the Command FIFO with data to transmit	This provides a buffer of 8 data bytes before transmission starts, so that the host does not need to write data as promptly for the rest of the burst
Write $0042 to Modem Mode and Control - $6B write	Start transmission	Initiates a transmission with preamble, Frame Sync 1 and then the pre-loaded data
IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait until the data block has been read from the FIFO	When this is complete a further 8 data bytes may be written to the Modem Command FIFO Data Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write) and the IRQ Status - $7E read register read again. This step may be repeated as many times as needed.
Write $F000 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Indicate burst end is intended	Indicate that no more data is to follow – so when the data loaded into the Command FIFO is modulated the CMX7364 will terminate the burst with tail bits
IRQ Status - $7E read register for bit 9 – Tx Last Tail = 1	Wait until the burst ends	The burst has completed, with all data and tail bits having been modulated. It is now possible to transition to other modes, or transmit another burst using the Modem Mode and Control - $6B write register.

The procedure described above can be adapted, making transmission of different numbers of bytes, bits or coded blocks possible.

Basic Receive Operation

Reception of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $8000 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous data reception
Write $1400 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 4 byte data block reception – repeat forever	Selects blocks of data bytes to be received (after frame sync is detected) – 4 bytes in each, at which point the host will be notified. This will continue until the mode is changed.
Write $0033 to Rx Tracking - $66 write	Select tracking modes	Selects automatic I/Q dc offset correction and symbol timing tracking
Write $0401 to Modem Mode and Control - $6B write	Start reception	Initiates a frame sync search, searching for Frame Sync 1. Once it is detected then Rx data will be made available.
-	Apply input signal	The input signal should contain preamble, Frame Sync 1 and then raw data. The frame sync should be detected and Rx data made available
IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait for data	This indicates that the 4 data bytes requested have been received and are available
Read the Receive FIFO Data Byte (see Receive FIFO Data/Control - $4C, $4D, $4E read) 4 times	Retrieve the received data	Data is read from the Receive Data FIFO. Once 4 data bytes are read the IRQ Status register may be read again to check if more data is available if required, and then those data bytes read. This step may be repeated as many times as needed
-	End of reception	Once enough data has been received a mode change (using the Modem Mode and Control - $6B write register) will stop reception or start searching for another frame sync.

The procedure described above can be adapted, making reception of different numbers of bytes, bits or coded blocks possible. The registers used for basic transmission and reception are:

- 10.1.19 Modem Mode and Control - $6B write
- 10.1.38 IRQ Status - $7E read
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.27 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.4 FIFO Control - $50 write
- 10.1.16 Rx Tracking - $66 write

7.4.3 Device Configuration (Using the Programming Register)

While in Idle mode the Programming register becomes active. The Programming register provides access to the Program Blocks. Program Blocks allow configuration of the CMX7364 during major mode change. Features that can be configured include:

- Flexible selection of Baud rates
- Pre-amble and frame syncs to be using in transmit and receive
- Selection of Automatic control of 4 x GPIO and the RAMDAC during transmission
- Configuration of RAMDAC profile
- Configuration of RSSI averaging
- Configuration of the carrier sense window and thresholds
- Configuration of System Clock outputs
- Configuration of SPI Thru-Port rate and word format
- Configuration of AGC commands using the SPI Thru-Port

Full details of how to configure these aspects of device operation are given in section 10.2 in the User Manual.

7.4.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of Idle mode. Configuration of the following features is possible:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Output gain
- Output dc offsets
- Selection of AGC mode, or manual control of the gain level.

The registers that allow configuration of these features are:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.22 I/Q Input Coarse Gain - $B1, $B2 write
- 10.1.24 I/Q Output Coarse Gain - $B4, $B5 write
- 10.1.23 I/Q Output Configuration - $B3 write
- 10.1.21 I/Q Input Configuration - $B0 write
- 10.1.5 AuxADC1-4 Control - $51 to $54 write
- 10.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 10.1.10 Signal Control - $61 write
- 10.1.15 AGC Control - $65 write

7.4.5 Interrupt Operation

The CMX7364 can produce an interrupt output when various events occur. Examples of such events include detection of a frame sync, an overflow of the internal data buffering in receive, or completion of transmission whilst in transmit.

Each event has an associated IRQ Status register bit and an IRQ Mask register bit. The IRQ Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the IRQ Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the IRQ Status register reflects the IRQN line state.

All interrupt flag bits in the IRQ Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. See:

- 10.1.38 IRQ Status - $7E read
- 10.1.20 IRQ Mask - $6C write

7.4.6 Signal Control

The CMX7364 offers two signal inputs (I Input, Q Input), and two modulator outputs (I Output, Q Output). The analogue gain/attenuation of each input and output can be set individually.

During I/Q modulation transmit, I Output and Q Output will output in-phase and quadrature output signals. They may be independently inverted and their gains changed. During I/Q modulation receive, I Input and Q Input will accept in-phase and quadrature modulated signals. They may be independently inverted and their gains changed.

During two-point modulation transmit the device will output two signals that may be used to drive VCOs in order to create FM modulation. The two signals are provided on the I and Q Outputs, they may be independently inverted and their gains changed.

Note: When transmitting (or receiving) in I/Q mode it may be necessary to swap the I and Q signals. This effect can be achieved by negating either the I or Q signals.
See:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.24 I/Q Output Coarse Gain - $B4, $B5 write
- 10.1.23 I/Q Output Configuration - $B3 write
- 10.1.21 I/Q Input Configuration - $B0 write

7.4.7 Tx Mode

In typical Tx operation, the preamble and FS1 or FS2 are transmitted automatically, and then data from the Command FIFO is transmitted directly until a TxEnd command is processed, or the mode is changed to Rx or Idle. Data may be written to the Command FIFO prior to starting transmission, enabling the host to create a buffer of data and therefore avoiding risk of the data running out during transmission. Further buffering is provided to expand the amount of data that may be absorbed by the CMX7364.

The host should write the initial data to the Command FIFO and then set modem control to the required transmit type with the Mode bits as Tx. As soon as the data has been read from the C-BUS TxData registers the Cmd Done IRQ and/or Command FIFO IRQ will be asserted (when configured correctly). More data should be loaded into the Command FIFO at this stage before data buffered in the CMX7364 runs out, otherwise an under-run will occur. To end the burst the host should send a TxEnd command, signalling to the CMX7364 that the burst is to end, and the imminent data under-run is intentional.

It is possible to define a transmission sequence with defined RAMDAC ramp up/down, and GPIO on/off events. The transmission sequence is configured using Program Block 5. For precise control of the instant that transmission starts it is possible to trigger a transmission using GPIOA as an input. Selecting a Tx mode with GPIOA configured as an “automatic input” places the device into a “Tx pending” state, where it is neither receiving nor transmitting, just waiting for a trigger on GPIOA to begin transmission.

In general Figure 15 describes operation when a transmit sequence is defined by the host by:

- Removing the need for the host to provide a ramp up – instead the configured Tx sequence will deal with this
- Inserting GPIO on/off events before ramp up and after ramp down as specified by the transmit sequence.

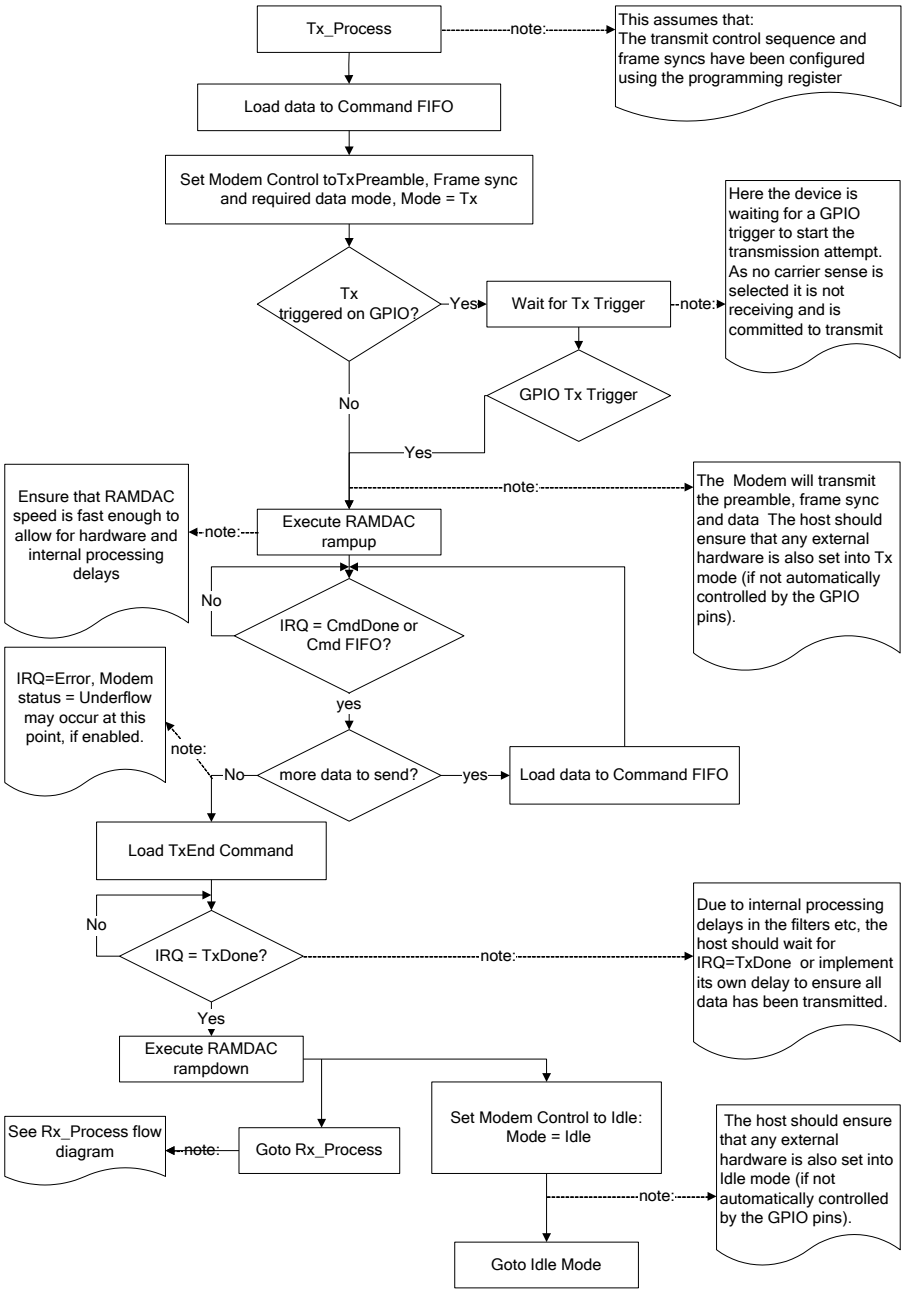


Figure 15 Host Tx Data Flow (No Tx Sequence/Carrier Sense)

7.4.8 Rx Mode

In Rx mode a frame sync must be detected, then data is supplied to the host through the Rx Data FIFO. Data should be read in response to a “Cmd Done”/”Rx Data FIFO” IRQ or status indication. The CMX7364 will continue decoding the input waveform until the host sets the mode bits to either Tx or Idle, as required. Once initial timing is established, timing corrections can be derived from the data to track the received signal. The Rx Tracking register allows selection of the tracking mode used to track the signal level, I/Q dc offset and symbol timing of the input signal as required. Use of the automatic tracking modes is recommended.

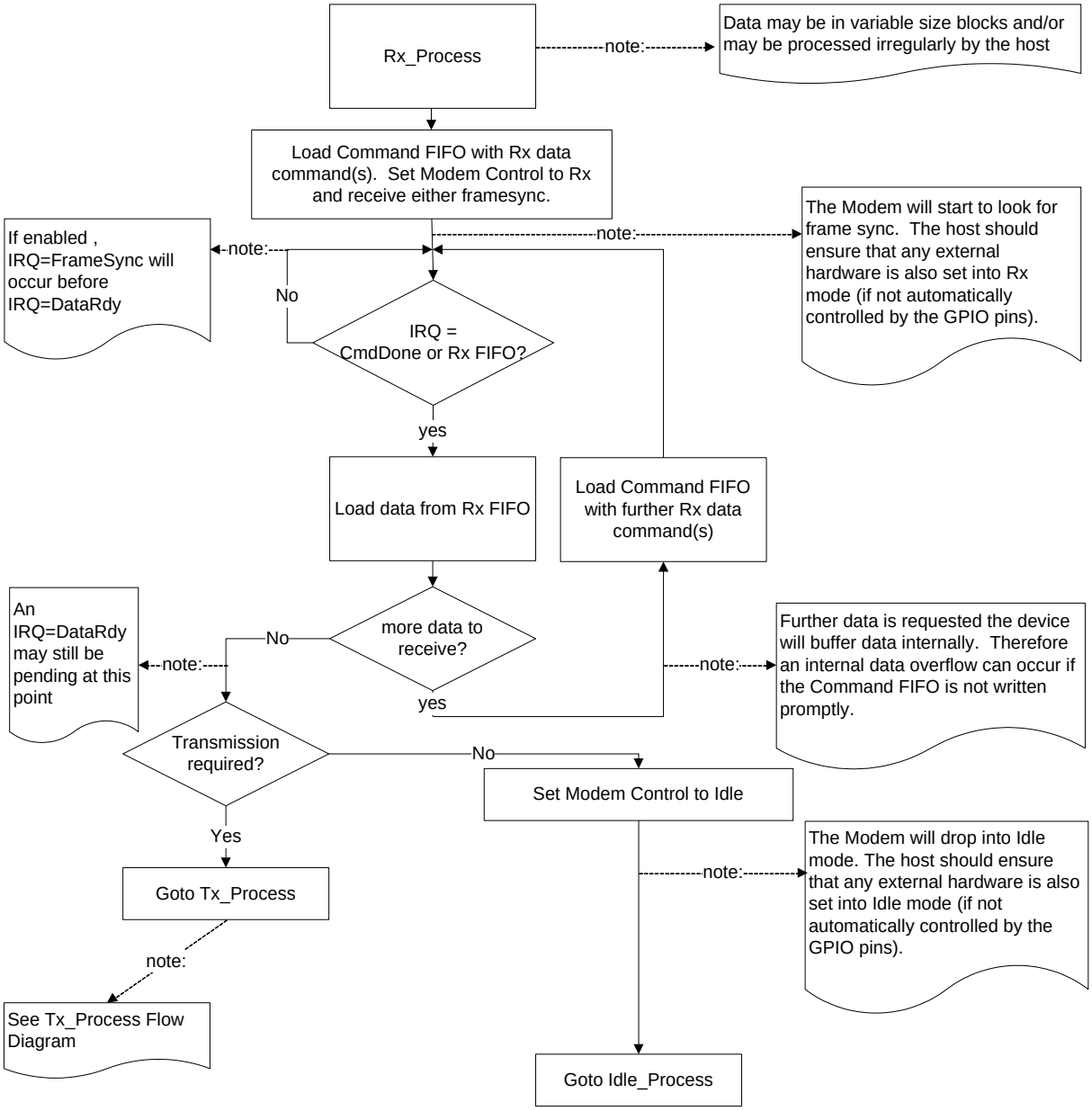


Figure 16 Host Rx Data Flow

7.4.9 Carrier Sense Mode

Carrier sense mode is a receive mode, pending a transmission. A carrier sense period, averaging window length and threshold must be defined in the Program Blocks prior to entering this mode. The signal strength is calculated internally – as the I/Q signal contains amplitude information.

On entry to Carrier Sense mode, reception will begin (or continue if the previous mode was receive) with an attempt to search for a frame sync. During the defined carrier sense period average RSSI will be computed over a moving window. Three outcomes are possible:

1. If during the carrier sense period the average RSSI is above the carrier sense threshold then transmission will be aborted, and search for frame sync will continue. The device reverts to receive.
2. There is a possibility that a valid frame sync will be detected during the carrier sense period. If this is the case, the transmission will be aborted immediately and the device will revert to receive.
3. If the RSSI average remains below the carrier sense threshold then transmission will proceed.

In each of the three possible cases, status bits will be used to indicate the result of the carrier sense period.

If the carrier sense mechanism is used in conjunction with GPIOA as a Tx trigger, operation is as follows: the device is put in receive, searching for a frame sync. If frame sync is found during this period then it is indicated to the host via the status bits and normal reception resumes. No carrier sense happens until GPIOA is used to start the transmit process, at which point carrier sense begins and operation is as described above.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7364 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

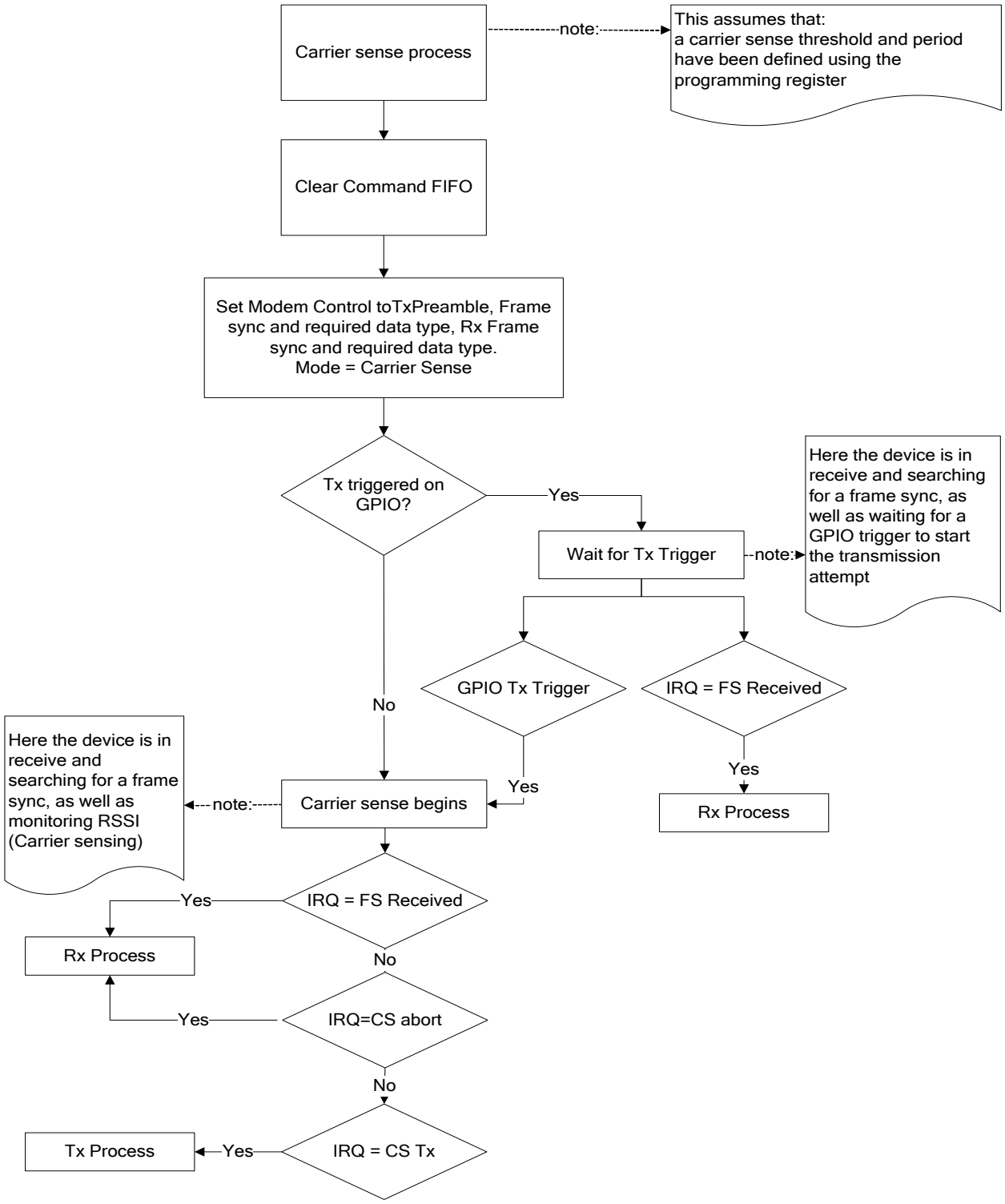


Figure 17 Carrier Sense

7.4.10 The Transmit Sequence

The CMX7364 is capable of being configured to provide the following features:

1. Selecting Tx mode results in transmission starting directly on entry to Tx mode or is delayed until GPIOA is used as an input trigger
2. Selecting carrier sense mode will result in behaviour as in point 1, followed by a carrier sense period, where transmission is delayed (reception continues) until a carrier sense period is completed and no activity is sensed on the channel
3. Selecting Tx calibration will cause CMX998 cartesian loop dc calibration to be carried out prior to transmission, as part of the programmable transmit sequence. See section 7.4.11 CMX998 DC Offset Calibration for details.
4. Once started, transmission can be configured to be a simple modulation output or can include a programmable sequence of events including RAMDAC ramp up/down and GPIO On/Off.

   Each of these operations can be selected independently of the others. The following diagram illustrates transmit operation.

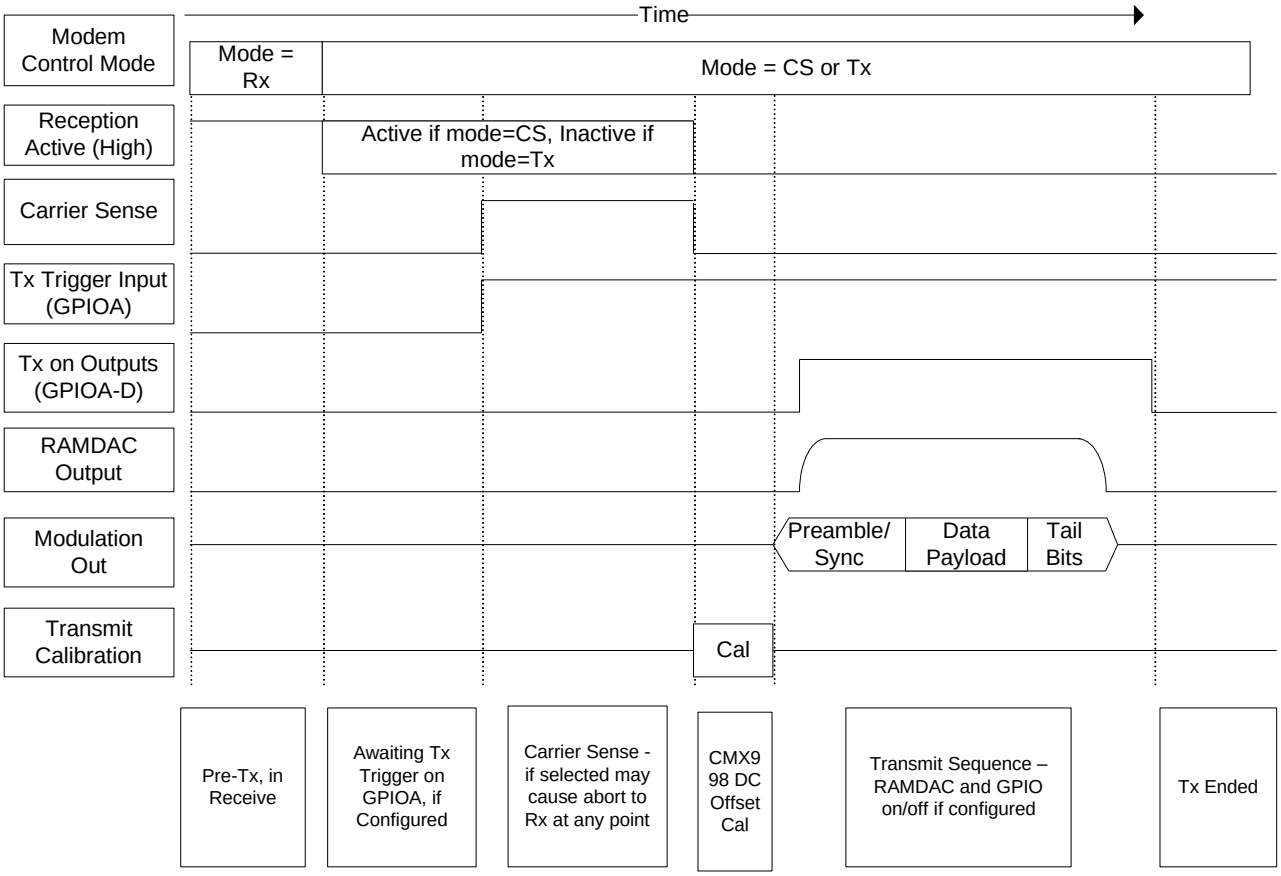


Figure 18 Transmit Sequence

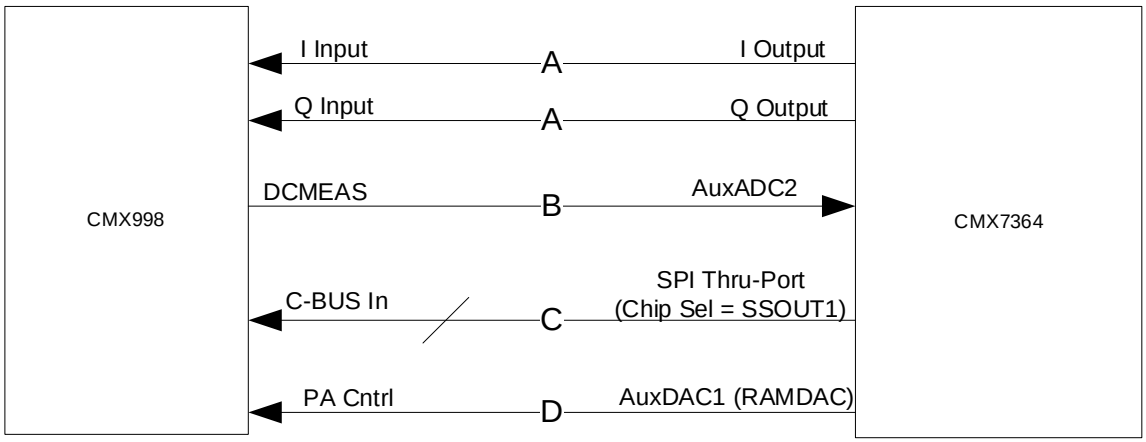
7.4.11 CMX998 DC Offset Calibration (I/Q Transmit Only)

When transmitting in I/Q mode, the CMX7364 may be interfaced to a CMX998 Cartesian Loop IC. The CMX998 is used to provide linearisation of the power amplifier used to transmit the modulation produced

by the CMX7364. If the signal produced by the CMX7364 when no modulation is present does not exactly match the dc reference of the CMX998, carrier leakage will result. This worsens the transmitted signal quality. DC offset calibration is intended to significantly reduce the carrier leakage.

The CMX998 Cartesian Feedback Loop Transmitter datasheet and an application note "CMX998 Cartesian Feedback Loop DC Calibration" are both available from the CML website (www.cmlmicro.com) and should be referred to for a more in-depth understanding of the need for dc offset calibration.

The CMX7364 performs automatic dc offset calibration as either part of a transmit sequence or in a separate calibration stage. DC offset calibration determines the dc offset that should be applied to the I Output and Q Output signals by the CMX7364 to minimise carrier leakage. The results of calibration will be held by the CMX7364 for use in later transmissions and are made available to the host. The interface is required to be as shown in Figure 19 CMX998 DC Calibration Interfaces.



A. The CMX7364 I and Q Outputs are used to provide dc levels, which are adjusted to make the error I/Q measurements equal to the Reference I/Q measurements

B. AuxADC2 is used to sample DCMEAS – To measure Reference signals and error signals

C. The SPI Thru-Port is used to control the CMX998 – selecting Reference I/Q and Error I/Q as measurements, as well as high gain/low gain modes of the CMX998

D. The RAMDAC is typically used to ramp-up the PA Control voltage after calibration is complete. This is not a part of the calibration sequence, but may be active as part of the transmit sequence.

Figure 19 CMX998 DC Calibration Interfaces

During calibration the CMX998 is controlled by the CMX7364 using the SPI Thru-Port chip select SSOUT1 to select one of the following to be output at the CMX998 DCMEAS pin:

I Reference	The CMX998 dc reference for the in-phase signal path
Q Reference	The CMX998 dc reference for the quadrature signal path
I Error (Low/high gain[2])	The CMX998 measure of the dc produced by the input signal on the in-phase signal path
Q Error (Low/high gain)	The CMX998 measure of the dc produced by the input signal on the quadrature signal path.

[2] The low and high gain states are created by adjusting the gain of the error amplifiers in the CMX998, see the CMX998 datasheet for more information.

During calibration the CMX7364 uses AuxADC2 to measure Reference I and Reference Q. It then puts (outputs) a dc level on the I Output, Q Output signals. AuxADC2 is used to measure the DCMEAS I and Q Error and I Output, Q Output are adjusted to make the DCMEAS I and Q errors equal to the DCMEAS I Reference and Q Reference measurements.

There are three complications to this process:

1. The total gain of the feedback loop I Output to CMX998 DCMEAS Error signal to AuxADC is unknown – so the adjustment to the I Output signal may not be calculated completely accurately from a single measurement. Therefore the gain applied to the calculated adjustment may be programmed and a number of iterations selected, resulting in a damped feedback loop.
2. The dc error to be corrected is usually large enough that if measured with the CMX998 in high gain mode the DCMEAS output would saturate. This makes calculation of the magnitude of error impossible. Therefore low gain mode should be used initially.
3. When changing from low to high gain modes the circuit changes (see dc calibration Application Note “CMX998 Cartesian Feedback Loop DC Calibration”), therefore the correction needed changes. However the low gain correction should at least be close to bringing the high gain measurement out of saturation. The relationship between correction computed using low gain and high gain is consistent – so may be noted and applied as an offset.

The calibration sequence implemented in the CMX7364 has the following stages:

Setup	Initialise the SSP port, AuxADC and select RefI as DCMEAS output from the CMX998
RefI	Read RefI, select DCMEAS = RefQ
RefQ	Read RefQ, select DCMEAS = ErrorI
ErrorILo	Read ErrorI assuming Low gain and adjust the I Output accordingly
ErrorQLo	Read ErrorQ assuming Low gain and adjust the Q Output accordingly
	Iterate – go to ErrorILo after a delay for corrected signals to settle
HighGain	Select High gain mode of the CMX998, apply Low to High gain mode correction
ErrorQHi	Read ErrorQ assuming High gain and adjust the Q Output accordingly
ErrorIHi	Read ErrorI assuming High gain and adjust the I Output accordingly
	Iterate – go to ErrorQHi after a delay for corrected signals to settle
Tidyup	Restore the CMX998, to its stage pre-calibration – ready to output modulation.

Note: Despite no modulation being produced, the Tx Done flag of the IRQ Status - $7E read register will be set at the completion of the CMX998 DC Offset Calibration task.

The timings of each calibration step can be configured using Program Block 5 – Burst Tx Sequence. To reduce calibration time, a calibration sequence may be configured that omits some stages of the calibration process. However there must always be a Setup and TidyUp stage, and if ErrorQHi and ErrorIHi are included then the high gain stage must be included as well.

The registers used during Tx dc offset calibration are:

- 10.1.19 Modem Mode and Control - $6B write
- 10.2.7 Program Block 5 – Burst Tx Sequence
- 10.1.31 I/Q Offset - $75, $76 read
- 10.1.8 I/Q Output Control - $5D, $5E write

7.4.12 Other Modem Modes

Tx Preamble
In Tx mode, a transmit preamble feature is provided to aid setup – the preamble may be programmed to any useful repeating 8-bit pattern.

Tx PRBS
In Tx mode, a fixed PRBS (pseudo random bit sequence) or a repeated preamble transmission is provided and may be used for test and alignment. A 511 bit PRBS conforming to ITU-T O.153 (Paragraph 2.1) is used to generate the PRBS.

Likewise the transmitted eye diagram when using 7364FI-8.x in two-point modulation 4-FSK mode is shown in Figure 20.

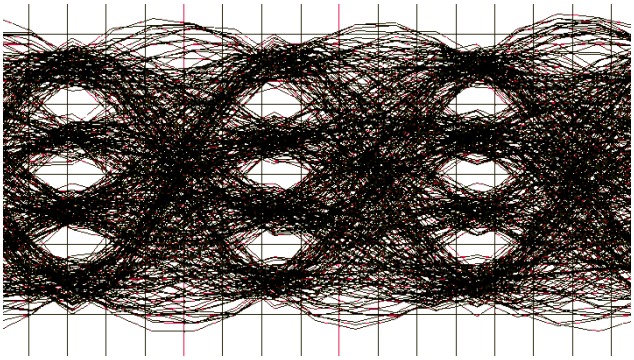


Figure 20 Transmit Eye Diagram

Rx Eye

A test mode to examine the Rx eye diagram is provided. This utilises the IOUTPUTP/N pins to produce a diagnostic output signal that may be used to create an eye diagram. The diagnostic signal is produced by channel filtering the I/Q input signals, FM demodulating the result and applying an Rx pulse shaping filter. This produces a one-dimensional eye diagram when displayed on an oscilloscope. One of the CMX7364 GPIO pins may be used as an oscilloscope trigger signal that is locked to the nominal Rx symbol rate, in order to display an eye diagram. For details on how to select the GPIO that produces a nominal symbol rate output clock signal and also the specific diagnostic mode see section 10.1.10 Signal Control - $61 write, Select b15-12=0011. Note that best results are often obtained with an analogue oscilloscope.

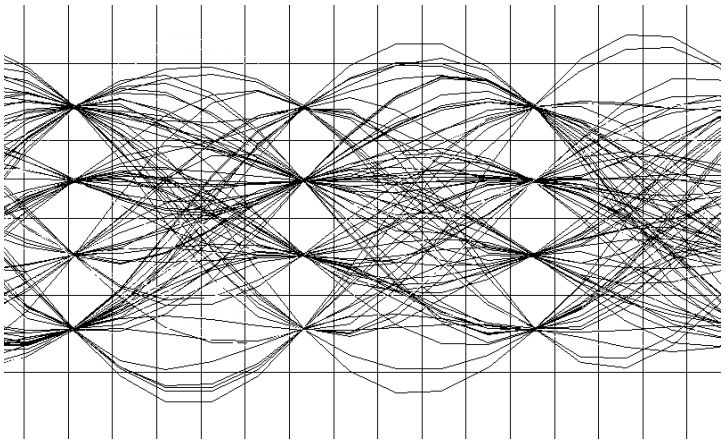


Figure 21 Received Eye Diagram

Rx Diagnostics

A diagnostic mode is provided that produces channel filtered I/Q signals and an optional dc offset correction indication. This aids in diagnosing reception issues that may be related to I/Q dc offsets in the CMX7364 input signal. As shown in Figure 22 and Figure 23, the estimated I/Q dc offset correction is an extra dot in the centre of the constellation.

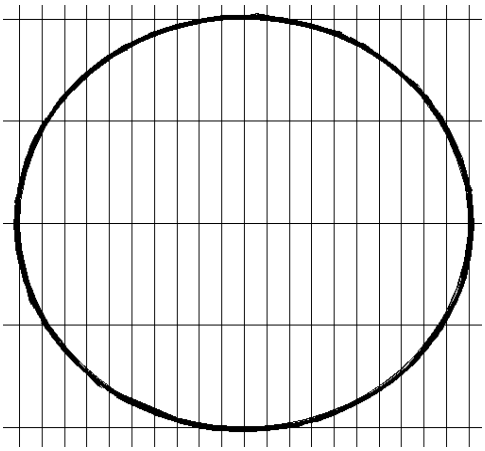


Figure 22 Channel Filtered I/Q Signals

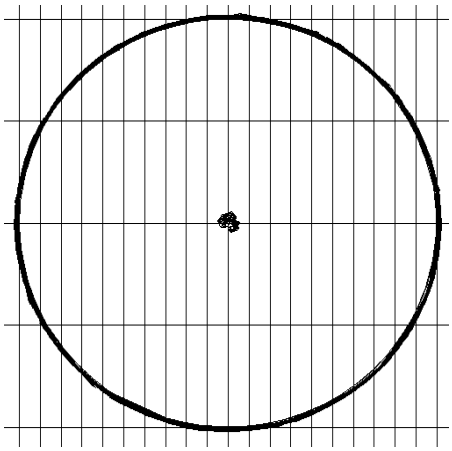


Figure 23 Channel Filtered I/Q Signals with I/Q DC Offset Estimate

Note: The images of receive diagnostic modes shown above are idealised. In practice when using the I Output and Q Output signals to view diagnostics the transitions between constellation point are not instantaneous. Using an analogue oscilloscope is the best way to observe these diagnostic signals.

See:

- 10.1.19 Modem Mode and Control - $6B write
- 10.1.10 Signal Control - $61 write.

7.4.13 Data Transfer

The payload data is transferred to and from the host via the C-BUS Command and Rx Data FIFOs, each of which provide efficient streaming C-BUS access. FIFO fill level can be determined by reading the Receive FIFO Level and Modem Command FIFO Level and controlled using FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached, or successful transfer of a block of host requested FIFO data between CMX7364 modem and FIFOs.

Each FIFO word is 16 bits, with the least significant byte (LSByte) containing data, and the most significant (MSByte) containing control information. The control information indicates to the CMX7364 what type, or how much data is in the LSByte. The control and data bytes may be written or read together using the Receive FIFO Word and Modem Command FIFO Word registers, or individually using their byte-wide registers.

Word wide FIFO writes involve writing 16-bit words to the Modem Command FIFO Word register using either a single write or streaming C-BUS. The whole word written is put into the Command FIFO, with the upper byte interpreted as control and the lower byte as data. This causes the control byte to be held in the Command FIFO Control Byte register.

Byte wide FIFO writes involve writing to the Modem Command FIFO Data Byte register using either single access or streaming C-BUS. This causes the Modem Command FIFO Control Byte (MSByte) and data written to the Modem Command FIFO Data Byte (LSByte) registers to be put into the command FIFO as one word. The control byte can be written separately as a single byte (this does not result in anything being added to the FIFO) or is preserved from a previous 16-bit Modem Command FIFO Data Byte write.

Likewise a word read from the Rx Data FIFO will return the Receive FIFO Control Byte in the MSByte and the Receive FIFO Data Byte at the top of the FIFO in the LSByte. Both registers will be updated so that when read next time they will provide details of the next item in the FIFO. Reading the Receive FIFO Control Byte only will not change the FIFO content. Reading the Receive FIFO Data Byte only will provide the data and remove the item from the FIFO – updating both control and data registers.
In summary:

Operation	Effect
write Modem Command FIFO Control Byte register	Cmd FIFO control word updated, nothing added to Cmd FIFO
write Modem Command FIFO Data Byte register	Cmd FIFO control word + data byte written are added to Cmd FIFO
write Modem Command FIFO Word register	data word (control and data bytes) is added to Cmd FIFO. Cmd FIFO control word updated for future writes.
read Receive FIFO Control Byte register	Rx FIFO control word is returned, no effect on Rx FIFO contents
read Receive FIFO Data Byte register	Oldest Rx FIFO data byte is removed from FIFO and returned, Rx FIFO Word updated
read Receive FIFO Data Word register	Oldest Rx FIFO data word (control and data bytes) is removed from FIFO and returned, Rx FIFO control word updated.

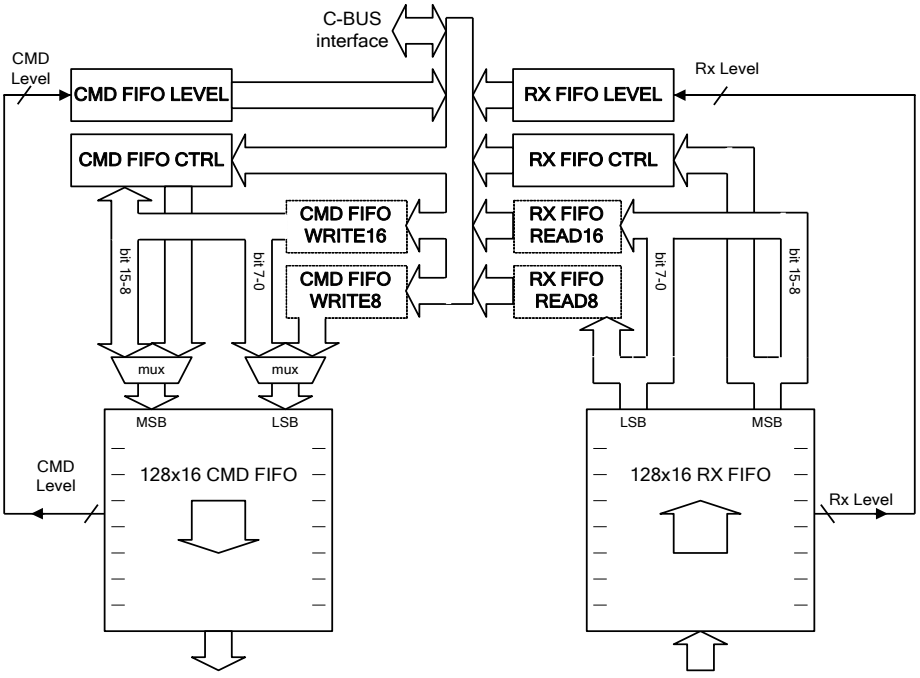


Figure 24 Command and Rx Data FIFOs

Raw or formatted data may be transmitted with the CMX7364 adding preamble, frame sync and tail bits. Raw or formatted transmission/reception is selected using the Modem Mode and Control - $6B write register, each whole transmission/reception must continue in the selected mode. Relevant registers are:

- 10.1.19 Modem Mode and Control - $6B write
- 10.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 10.1.27 Receive FIFO Data/Control - $4C, $4D, $4E read
- 10.1.26 Modem Command FIFO Level - $4B read
- 10.1.28 Receive FIFO Level - $4F read
- 10.1.4 FIFO Control - $50 write

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7364 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.14 Data Buffering

To expand the buffering capabilities of the CMX7364 two internal buffers are provided:

A Command buffer which buffers commands from the control FIFO which are yet to be processed.
An Rx data buffer which buffers received data yet to be loaded into the Rx data FIFO.

Transfer between the FIFOs and their respective buffers will occur during transmission, reception and Idle mode. Such transfer is not instantaneous so the FIFO fill levels should be used to indicate how much data the host may read or write at any time.

The Internal Buffer Fill Level - $70 read register allows the buffer fill levels to be read; their contents will be flushed when the respective FIFO is flushed.

See:
- 10.1.4 FIFO Control - $50 write
- 10.1.29 Internal Buffer Fill Level - $70 read.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7364 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.15 Raw Data Transfer
When transferring raw data the FIFO Control byte indicates the amount of data that will be transferred in a block before the CMX7364 interrupts the host. Byte and bit-wise transfers are possible, providing the facility to transmit or receive a burst of arbitrary length, not just a whole number of bytes. It is suggested that data is transferred in the maximum size blocks possible until the end of a burst – where the remaining bits, or bytes can be transferred in a single transaction of the required size.

When using byte wise transfers the most significant bit of the data byte is transmitted (or received) first. In The bits are combined into symbols according to the selected modulation type.

It is also possible to ignore the concept of blocks of data whilst in raw mode. Instead, a transmission can just be treated as a series of bytes to transmit and FIFO levels/level IRQs used to manage the data flow. Likewise in receive the host can request continual data reception and the resulting bytes will be placed in the Rx Data FIFO. FIFO levels and level IRQs may be used to manage the data flow. This mode provides the ability to simply stream (using streaming C-BUS if desired) multiple bytes into or out of the CMX7364 as FIFO content allows.

7.4.16 Formatted Data Transfer
When the transfer of formatted data is selected by the Modem Mode and Control - $6B write register the FIFO Control byte indicates the RTCM SC135 frame type to use in either sending or decoding the data. The frame type dictates the format or quantity of data transferred, including how error detection and correction bits are added to the over air data stream.

7.4.17 Pre-loading Commands
It is advisable to pre-load data into the Command FIFO before transmission begins, or to pre-load receive data commands into the Command FIFO prior to frame sync reception.

7.4.18 GPIO Pin Operation
The CMX7364 provides four GPIO pins, each pin can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input function which is only allowed for GPIOA).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC – AuxDAC1 (if it is configured as automatic) during the course of a burst. Pins that are manual are under direct user control. When automatic, a rising or a falling event at the start or end of transmission will cause the specified GPIO to be switched high or low accordingly.

GPIOA may be configured as an automatic input. This means that any attempted transmission will wait until GPIOA input is high (if rising is selected) or low (if falling is selected).

See:
- 10.2.7 Program Block 5 – Burst Tx Sequence
- 10.1.14 GPIO Control - $64 write
- 10.1.34 GPIO Input - $79 read.

7.4.19 Auxiliary ADC Operation

The inputs to the four Auxiliary ADCs can be independently routed from any of four dedicated AuxADC input pins or the two main inputs. AuxADCs can be disabled to save power. BIAS in the VBIAS Control - $B7 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC1-4 Control - $51 to $54 write registers. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in the AuxADC1-4 Control - $51 to $54 write registers. Setting the average counter to zero will disable the averager, for an average value of 1; 50% of the current value will be applied, for a value of 2 = 25%, 3 = 12.5%, continuing up to the maximum useful value of 11 = 0.0488%.

High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when an input exceeds the high or low threshold, or on every sample as required. The thresholds are programmed via the AuxADC1-4 Threshold- $55 to $58 write register.

Auxiliary ADC data is read back in the AuxADC1-4 Read - $71 to $74 read registers and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is selected using Program Block 1 – Clock Control.

See:

- 10.1.5 AuxADC1-4 Control - $51 to $54 write
- 10.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 10.1.30 AuxADC1-4 Read - $71 to $74 read
- 10.2.3 Program Block 1 – Clock Control
- 10.1.25 VBIAS Control - $B7 write.

7.4.20 Auxiliary DAC/RAMDAC Operation

The four auxiliary DACs are programmed via the AuxDAC1-4 Control - $59 to $5C write registers. AuxDAC1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The RAMDAC may be configured as automatic or manual using Program Block 5 – Burst Tx Sequence. The AuxDAC1-4 Control - $59 to $5C write register, with b12 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC. The RAMDAC ramp rate is controlled by the Internal system clock rate, which changes between active CS/Tx/Rx modes and Idle mode. Therefore it is inadvisable to return to Idle mode prior to RAMDAC ramp completion.

The default profile is a Raised Cosine (see Table 5 in the user manual), but this may be over-written with a user defined profile by writing to Program Block 0. The current profile may be scaled using the Signal Control - $61 write register. The AuxDAC outputs hold the user-programmed level during a power-save operation if left enabled, otherwise they will return to zero.

See:

- 10.1.7 AuxDAC1-4 Control - $59 to $5C write
- 10.2.2 Program Block 0 – RAMDAC
- 10.2.3 Program Block 1 – Clock Control
- 10.2.7 Program Block 5 – Burst Tx Sequence
- 10.1.10 Signal Control - $61 write.

7.4.21 SPI Thru-Port (SSP)

The CMX7364 provides an SPI Thru-Port synchronous serial port (SSP) master interface that can perform transactions with up to three external slave SPI/C-BUS devices (0, 1 and 2) respectively selected via CMX7364 SSOUT0, SSOUT1 and SSOUT2 chip select output signals. In addition to those chip select signals the interface includes clock out (CLK), data out (MOSI) and receiving data in (MISO) signals shared by all connected slaves.

The Thru-Port supports independent, slave-specific operating characteristics via three configuration parameter sets in Program Block 6 – SPI Thru-Port Configuration. Some of the configurable characteristics are clock speed, inter-frame guard period, clock phase/polarity, and C-BUS/SPI transaction format. The CMX7364 automatically applies each slave's Program Block 6 Thru-Port Configuration characteristics in response to whichever external slave device will be selected by CMX7364 SSOUT0, SSOUT1 or SSOUT2 chip select pins.

7.4.21.1 SPI Thru-Port (SSP) configuration conflicts

Note: Once a Thru-Port transaction with an external device has been initiated it must be allowed to complete before Thru-Port Configuration characteristics are changed otherwise the ongoing transaction may be corrupted. Accordingly the CMX7364 host driver must not cause a Thru-Port transaction to be initiated if that would cause a configuration conflict i.e. select a slave having a different Thru-Port Configuration characteristic than that of an ongoing transaction.

SPI Thru-Port transactions may be initiated by the following methods.

1. Host Single Thru-Port Commands – The CMX7364 host writes a C-BUS command to the SPI Thru-Port Control - $62 write register (section 10.1.11) after having optionally written associated data to the SPI Thru-Port Data Write1 - $63 write (section 10.1.12) register. If this initiates a Thru-Port read transaction then when that completes any returned data read is reported in the CMX7364 SPI Thru-Port Data Read - $78 read (section 10.1.33) register, from where the host may read it via C-BUS transaction. This Thru-Port transaction method executes a single Thru-Port transaction with one serial slave. The host driver must pace when it issues Host Single Thru-Port Commands so they do not cause a Thru-Port configuration conflict.
2. SSP Macro Thru-Port Commands – SSP macros each comprising a sequence of one or more SPI Thru-Port write transactions may be configured in Program Block 6 – SPI Thru-Port Configuration (section 10.2.8). An SSP macro may include Thru-Port transactions with multiple slave devices that have different SPI Thru-Port Configuration characteristics, in which case SSP macro execution automatically paces its own Thru-Port Configuration characteristic changes so they do not cause configuration conflicts amongst themselves. Execution of an SSP macro's Thru-Port transactions is initiated by writing to the Modem Mode and Control - $6B write with specific bits set; see section 10.1.19 for details.
3. Autonomous CMX998 Tx DC Calibration – While the CMX7364 modem is in Tx mode the device can optionally perform Tx DC Calibration of an external CMX998 transmitter device connected as the SPI Thru-Port slave selected by SSOUT1. The calibration process and its associated Thru-Port transactions are initiated by writing to the CMX7364 Modem Mode and Control - $6B write register; see section 10.1.19 for details.
4. Autonomous AGC Using SPI Thru-Port – As described in section 7.4.22 SPI/C-BUS AGC, while the CMX7364 modem is in Rx mode the device may autonomously perform Thru-Port transactions under the control of the CMX7364 AGC function in its Auto mode. In addition, while the AGC function is in its Manual mode and the CMX7364 modem is in any of Rx, Tx or Idle modes then a host C-BUS write that manually selects an AGC function gain step will initiate an associated Thru-Port transaction. Individual AGC Thru-Port transactions are configured in Program Block 7 – AGC Configuration (section 10.2.9) and could include multiple external slave devices having different Thru-Port Configuration characteristics. Accordingly, the configured timing of the AGC function and its associated Thru-Port transactions, whether associated with autonomous or manual AGC gain changes, must be arranged not to cause a Thru-Port configuration conflict.

The SSP Macro Thru-Port Commands, Autonomous CMX998 Tx DC Calibration and Autonomous AGC Using SPI Thru-Port methods initiate Thru-Port transactions by a host C-BUS write to the same CMX7364 Modem Mode and Control - $6B write register. The latter two require the CMX7364 modem to be in mutually exclusive modes (Tx and Rx) and so cannot be simultaneously initiated to mutually cause a Thru-Port configuration conflict. However, SSP Macro Thru-Port Commands and either Autonomous CMX998 Tx DC Calibration or Autonomous AGC Using SPI Thru-Port methods can be simultaneously initiated by the same C-BUS write to the Modem Mode and Control - $6B write register, which could cause a configuration conflict. The SSP Macro Wait feature, enabled on the same write to the Modem Mode and Control - $6B write register, avoids such a conflict by causing resulting Thru-Port transactions to sequence with the SSP Macro Thru-Port Commands performed first.

7.4.21.2 SPI Thru-Port C-BUS and SPI Transaction Modes

In order to offer a simpler, more convenient interface, a slave device's Thru-Port configuration can be designated C-BUS, rather than SPI. This means that data read/written is assumed to be in the format:

Address byte, data byte1 (optional), data byte 2 (optional)

In each case the CMX7364, as the master, drives the address and data for a write operation, or drives the address and receives the data for a read operation. Commands can be called 0, 1 or 2 byte reads or writes – with a 0 byte write typically being a reset command. As the word format is known, then for convenience only the desired read data is returned to the host.

SPI mode is more general and makes no assumption about the SPI word format or that its data field length is a whole number of bytes.

See:

- 10.1.11 SPI Thru-Port Control - $62 write
- 10.1.12 SPI Thru-Port Data Write1 - $63 write
- 10.1.33 SPI Thru-Port Data Read - $78 read
- 10.2.8 Program Block 6 – SPI Thru-Port Configuration.

7.4.22 SPI/C-BUS AGC

Using the SPI Thru-Port, the CMX7364 provides an AGC function that can control an external C-BUS or SPI device capable of implementing variable gain steps in the receive signal path. The state of a GPIO output can also optionally be configured to change with AGC function gain state and thereby control additional external hardware. The function's Auto modes act autonomously only while the modem is in Rx mode; when in manual mode the function acts in response to manual gain step selection while the modem is in any of Rx, Tx and Idle modes.

During receive, the AGC function can provide a fast-response gain reduction to large signals that cause clipping and a gain increase when the signal becomes too small. Controlling the external device requires the host to program a table of eight SPI/C-BUS commands that the CMX7364 stores and outputs when a specific gain step is required. In conjunction with each gain step that is output, a second external device can also be enabled using one of the four available GPIO pins. This feature is intended for use with RF systems using an external LNA or other stages prior to a SPI/C-BUS controlled device. The commands may be produced by the AGC function, or the CMX7364 can be commanded to output them manually if required. Commands are programmed using Program Block 7 – AGC Configuration.

By default the AGC function range is 8 gain selection steps, 0 to 7 with 0 being the lowest gain and 7 being the highest. If a range of fewer steps is desired then Program Block 7 – AGC Configuration can be used to set the lowest gain step that the AGC is allowed to select. For example, if the lowest allowed gain step is set to 4 the AGC will select AGC function gain steps 4 to 7 only.

AGC function state is controlled by sensing over-range in the CMX7364 received input signal – in which case the external gain is backed off. While searching for a frame sync, the gain will also be backed off when the signal is considered "large" – this ensures that after frame sync is detected there is headroom for the amplitude to increase a little. If the signal is sensed to be small for a period of time the gain can also be increased. The signal magnitude low or high threshold considered to require a gain change, the time for which it should remain low before making a change and the time to allow a gain adjustment to take effect are all programmable. The overall system is shown in Figure 25.

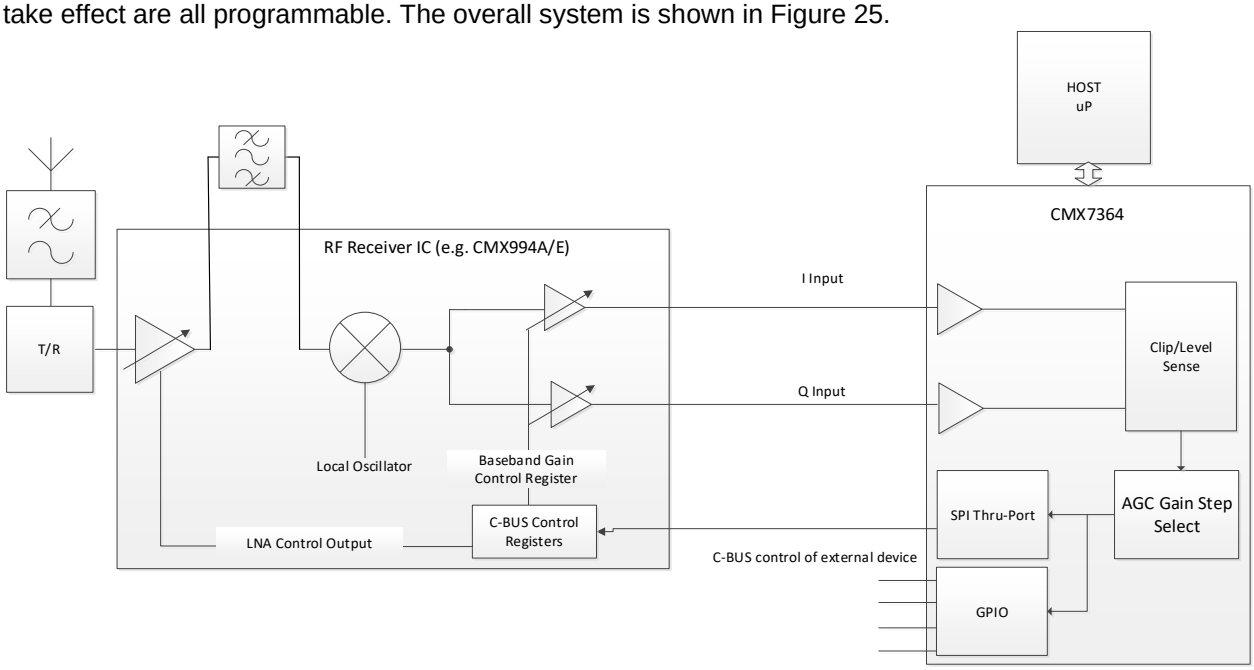


Figure 25 AGC using SPI Thru-Port

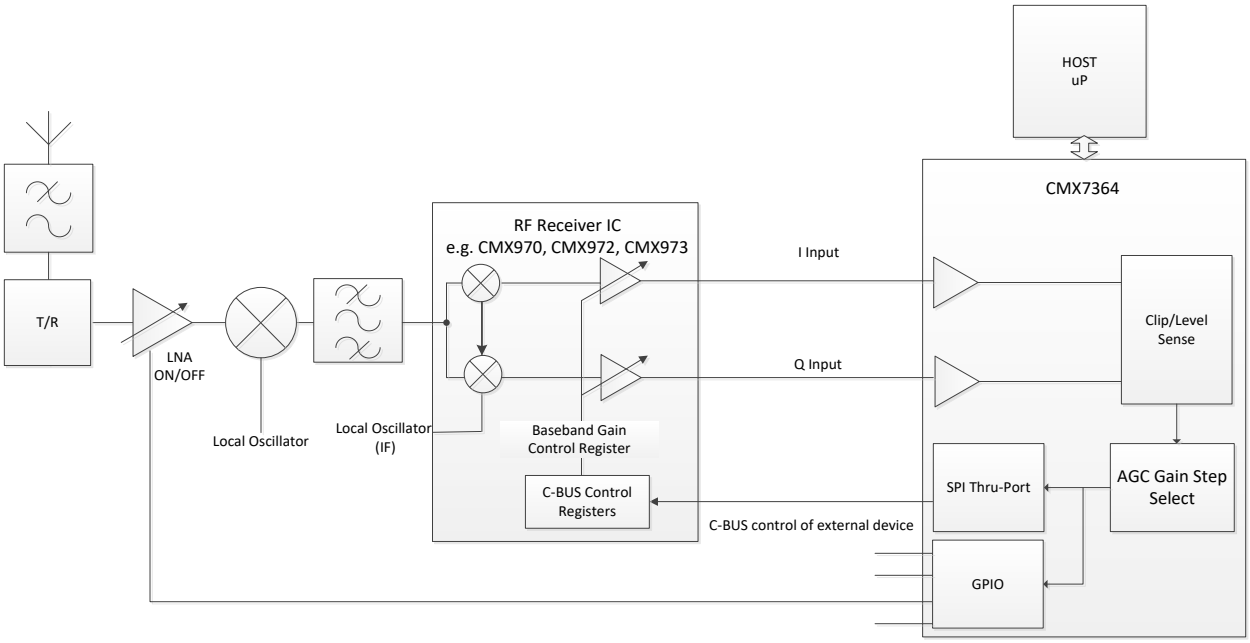


Figure 26 AGC using SPI Thru-Port and external LNA

Note: The external LNA control feature of the CMX7364 may be useful where an RF device does not provide an LNA control output like that available in the CMX991 or CMX992. An example of where CMX7364 control would be necessary is a receiver using the CMX994/A/E but not using the IC's internal LNA; in order to achieve the maximum operating dynamic range of a direct conversion receiver, like the CMX994/A/E, the signal level to mixers must be controlled in order to minimise the chance of local oscillator pulling hence the need for LNA control.

Controlling the external device as shown in Figure 25 causes the gain to step suddenly. This in itself may cause a short burst of errors, so once signal is being received it may be desirable to ensure that the gain is not changed unnecessarily. This is typically the case with short bursts of data, where it is likely that the signal amplitude will remain constant throughout the burst. To help achieve this, various AGC automatic modes are provided:

- Manual Gain – Controlled manually always, allowing user control and for control during latching in of I/Q dc corrections
- Full Auto – Gain can increase and decrease during the search for frame sync and during burst reception
- AGC lock on FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will be fixed
- AGC down after FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will only decrease.

AGC gain changes made during the frame sync section of the input signal introduce a signal amplitude distortion that can cause CMX7364 frame sync detection to fail. To avoid this the CMX7364 compares the incoming on-channel signal to a Signal Detect Threshold that when first exceeded is interpreted to indicate the start of an arriving burst i.e. the burst's preamble field. This event, the amplitude of the CMX7364 input signal before and after AGC gain changes and whether a frame sync is detected within a certain time causes the AGC function to change states according to configured AGC level and timing settings. State changes include reducing gain by one step (or optionally two if the input signal amplitude is high enough to cause clipping), increasing it by one step, not changing gain for a certain time (e.g. immediately after a gain change or when the frame sync field is expected to arrive), and returning to the

original starting state (e.g. if after the detect threshold was first exceeded no frame sync was detected within the maximum expected time). Some AGC behaviour is illustrated in Figure 27.

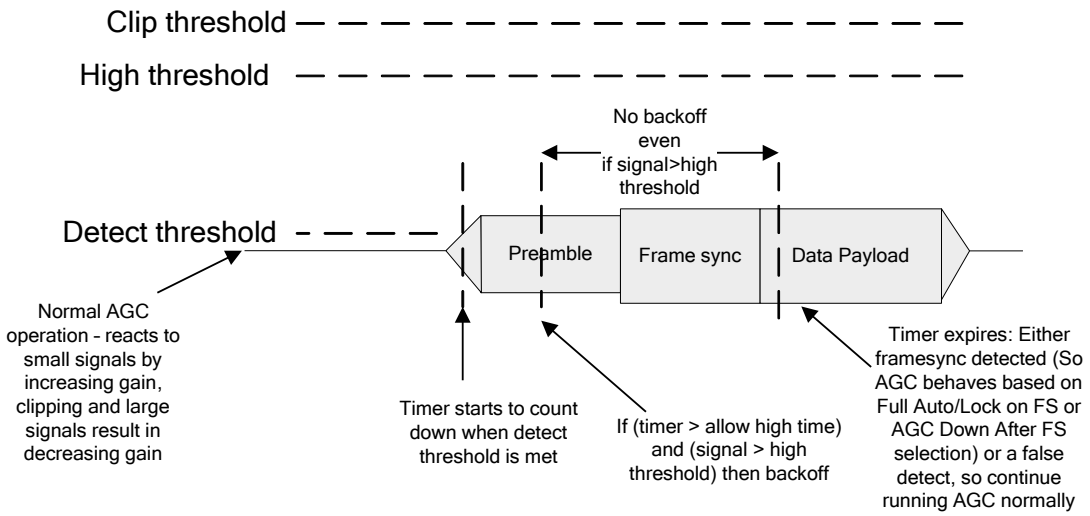


Figure 27 AGC Behaviour During Burst Reception

A general issue with I/Q receivers is that of dc offsets. Offsets are generated by the receiver hardware and typically vary with channel selection but depending on receiver architecture may also change with gain selection. The CMX7364 is capable of calculating I/Q dc offset corrections but if gain steps makes dc offset change suddenly then errors may occur. Once again this may only be an issue for longer bursts when it is necessary to change gain during reception.

To mitigate the dc offset change with gain change effect, the CMX7364 allows an I/Q dc offset correction for each AGC non-maximum gain step to be calibrated in advance and latched in for later application. (The dc offset corrections are applied during normal Rx operation so they must be calibrated while all normal operation dc offset contributors are active. The CMX7364 Rx Equaliser can contribute dc offset so if it will be used it must be properly trained before then operated with trained coefficients while calibrating the dc offset corrections.) Thereafter when a non-maximum gain AGC gain step is selected its corresponding tabulated dc offset correction will be applied. Additionally, receivers that present large dc offset may, when their gain is stepped, cause a sufficiently large dc offset change that makes the signal appear, to the AGC algorithm, smaller or larger than it actually is and thereby cause unwanted AGC gain changes.

AGC thresholds and parameters are controlled using the Signal Control - $61 write register and may be changed during reception for ease of setup. All times are measured in units of 6/5 of a symbol period. All levels or thresholds are compared to the magnitude of signed 16 bit samples, with max range therefore being 32767 to -32768.

Further description and operational scenarios are described in Application Note AT0674, available on the CML tech portal.

AGC Observe

The CMX7364 AGC function described above has several states. The current state is not externally observable during normal operation. It is determined by AGC function configuration in combination with the CMX7364 input signal history. Different states allow or prevent AGC function actions to change gain. To help users properly configure the AGC function, an AGC Observe function is provided and makes AGC function state and behaviour externally observable. AGC Observe indicates current AGC function state as a code value in an Aux ADC C-BUS register or a code voltage on an Aux DAC output pin. (While AGC Observe is enabled, the Aux DAC or Aux ADC C-BUS register selected for its use is not available for normal Aux DAC or ADC operation thus AGC Observe is intended to be used as a configuration design tool, not enabled during regular modem operation.) AGC Observe is activated and its Aux DAC or ADC output mode selected using Program Block 4 – Modulation Control. The table below lists AGC function states and their AGC Observe codes.

					Input Signal Case That Causes AGC Action		
	AGC Function State	Preamble detected	Frame sync detected	**AGC Observe Code** (value written to selected Aux ADC C-BUS register or instead to Aux DAC, which sets its output voltage)	ADC clipping	Above high threshold	Below low threshold
1.	Waiting for burst - active, with AGC function timers reset			$000	x	x	x
2.	Rx burst start detected	x		$100	x	x	x
3.	Preamble detected, no high threshold action thereafter option	x		$200	x		x
4.	Frame sync detected, no AGC action therafter option	x	x	$300			
5.	Frame sync detected, only AGC gain reduction action thereafter option	x	x	$380	x	x	
6.	Frame sync detected, any AGC action thereafter option	x	x	No update	x	x	x

Note: There is a short delay between when a signal is applied to the CMX7364 input pins and when it is sensed by the AGC. There is a longer delay (caused by the CMX7364 channel filter) before the frame sync is detected by the preamble and frame sync detectors.

See:

- 10.2.8 Program Block 6 – SPI Thru-Port Configuration
- 10.2.9 Program Block 7 – AGC Configuration
- 10.2.6 Program Block 4 – Modulation Control
- 10.1.15 AGC Control - $65 write
- 10.1.10 Signal Control - $61 write
- 11.2.1 Effect of AGC on DC Offsets

7.5 Digital System Clock Generators

The CMX7364 includes a two-pin Xtal Oscillator circuit. This can either be configured as an oscillator, as shown in section 4, or the XTAL/CLK input can be driven by an externally generated clock. The crystal (Xtal) source frequency is typically 9.6MHz and if an external oscillator is used, the input frequency is typically 9.6 or 19.2 MHz. For both cases reference frequencies in the range specified in 9.1.2 Operating Limits may be used.

7.5.1 Main Clock Operation

A digital PLL is used to create the main clock for the internal sections of the CMX7364. The configuration of the main clock and the internal clocks derived from it is controlled using Program Block 1 – Clock Control.

The CMX7364 defaults to settings appropriate for a 19.2MHz externally generated clock with a baud rate of 9.6ksymbols/s, however if a different reference frequency is to be used, or a different baud rate required, then Program Block entries P1.1 to P1.6 will need to be programmed appropriately at power-on. Preferred values are provided in **Error! Reference source not found.** and Table 6 along with details of how to calculate settings for other baud rates and crystal frequencies.

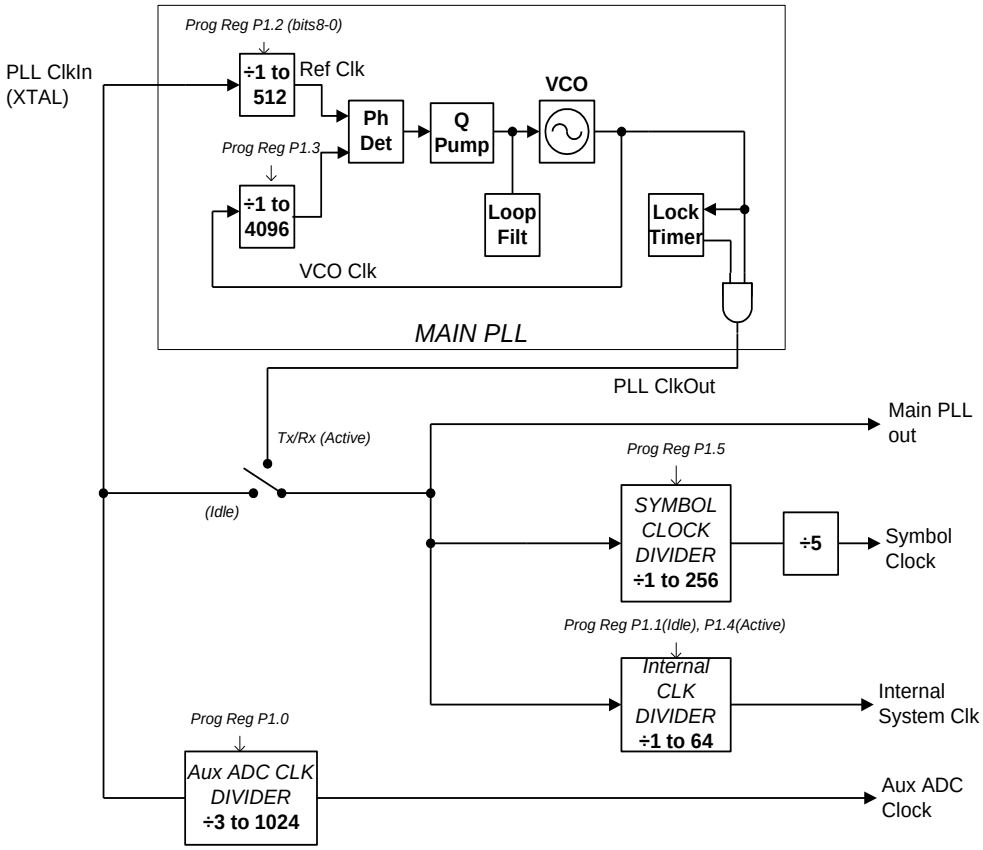


Figure 28 Main Clock Generation

See:

- 10.2.3 Program Block 1 – Clock Control.

7.5.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. The System Clock circuitry is shown in Figure 29 Digital System Clock Generation Schemes.

Having chosen the input frequency source, system clock generation may be by simply dividing the input frequency source, or via its own phase locked loop. The system clock PLL does not affect any other internal operation of the CMX7364 – so if a frequency that is not a simple fraction of the Xtal is required, it can be used with no side effects. There is one phase locked loop, with independent output dividers to provide phase locked output signals.

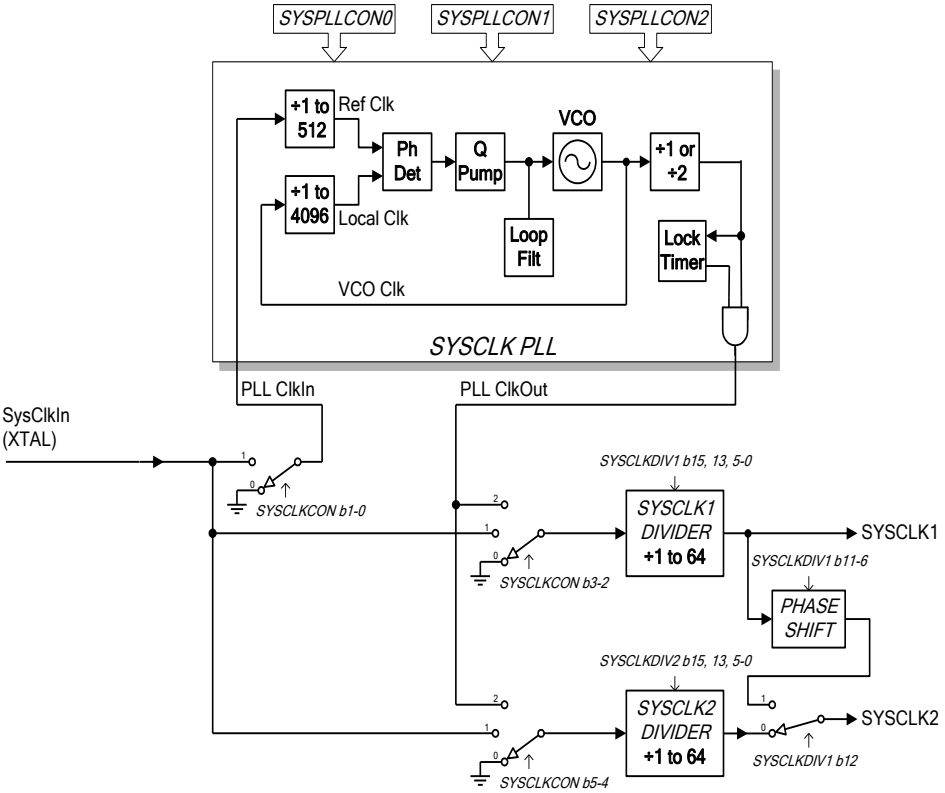


Figure 29 Digital System Clock Generation Schemes

See:

- 10.2.3 Program Block 1 – Clock Control.

7.6 Signal Level Optimisation

The internal signal processing of the CMX7364 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 9.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

7.6.1 Transmit Path Levels and Modulation Envelope Ramping

For the maximum signal out of the I/Q Outputs, the signal level at the output of the modem block is set to be 0dB, the Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The signals output from I Output and Q Output may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment. When transmitting I/Q format signals inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets may be added to the signal, however care must be taken that the combination of gain and dc offset does not cause the signal to clip at any point in the signal processing chain, which is: Fine gain followed by dc offset addition, followed by coarse gain.

The transmit I/Q output signal represents instantaneous modulation signal power, which determines the modulation envelope. For a given transmit burst, how quickly the I/Q signal envelope rises at burst start and declines at burst end can influence the resulting modulation signal spectrum; if the I/Q envelope makes a rapid step change the bandwidth associated with that transient step may be wider than desired.

The 4-FSK modulations produced are constant envelope so, by default, at burst start and end their transmit I/Q signal modulation envelope respectively steps from 0% to 100% and from 100% to 0%, without any inherent ramping effect. The modulation envelope can be optionally ramped up and down at beginning and end of a transmission. To select and configure this option see:

- 10.1.8 I/Q Output Control - $5D, $5E write
- 10.1.24 I/Q Output Coarse Gain - $B4, $B5 write
- 10.2.6 Program Block 4 – Modulation Control

7.6.2 Receive Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the I Input or Q Input pins is specified in section 9.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7364 should operate correctly with the default level selected. The primary purpose of the Fine Input level adjustment is to allow independent inversion of the I/Q Input signals. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment. When receiving I/Q format signals, inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets can be removed by the CMX7364, the offset to remove can be selected by the host or calculated automatically by the CMX7364.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal dc offset removal or attenuation.

See:

- 10.1.9 I/Q Input Control - $5F, $60 write
- 10.1.21 I/Q Input Configuration - $B0 write

7.7 C-BUS Register Summary

Table 1 C-BUS Registers

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)
$01	W	C-BUS General Reset	0
$48	W	Modem Command FIFO Data Byte	8
$49	W	Modem Command FIFO Word	16
$4A	W	Modem Command FIFO Control Byte	8
$4B	R	Modem Command FIFO Level	8
$4C	R	Receive FIFO Data Byte	8
$4D	R	Receive FIFO Word	16
$4E	R	Receive FIFO Control Byte	8
$4F	R	Receive FIFO Level	8
$50	W	FIFO Control	16
$51 to $54	W	AuxADC1-4 Control	16
$55 to $58	W	AuxADC1-4 Threshold	16
$59 to $5C	W	AuxDAC1-4 Control	16
$71 to $74	R	AuxADC1-4 Read	16
$5D	W	I Output Control	16
$5E	W	Q Output Control	16
$5F	W	I Input Control	16
$60	W	Q Input Control	16
$61	W	Signal Control	16
$65	W	AGC Control	16
$66	W	Rx Tracking	16
$69	W	Reg Done Select	16
$70	R	Internal Buffer Fill Level	16
$75	R	I Offset	16
$76	R	Q Offset	16
$77	R	AGC Gain and RSSI	16
$7A	R	Rx Error Magnitude	16
$7B	R	Frequency Error	16
$62	W	SPI Thru-Port Control	16
$63	W	SPI Thru-Port Write	16
$64	W	GPIO Control	16
$78	R	SPI Thru-Port Read	16
$79	R	GPIO Input	16
$6A	W	Programming	16
$6B	W	Modem Mode and Control	16
$6C	W	IRQ Mask	16
$7D	R	Programming Register Read	16
$7E	R	IRQ Status	16
$7F	R	Modem Mode and Control Readback	16
$B0	W	I/Q Input Configuration	16
$B1	W	I Input Coarse Gain	16
$B2	W	Q Input Coarse Gain	16
$B3	W	I/Q Output Configuration	16
$B4	W	I Output Coarse Gain	16
$B5	W	Q Output Coarse Gain	16
$B7	W	V_{BIAS} Control	16

All other C-BUS addresses are reserved and must not be accessed.

8 Features

The device uses a 4-FSK modulation scheme with a configurable over-air symbol rate of either 4.8 or 9.6 ksymbols/s, In each case, the modulating signal is root raised cosine filtered with a filter alpha of 0.2, followed by an optional sinc filter. Raw data can be transferred and, in addition, formatted data blocks following the RTCM SC135 standard are supported and may be of variable length (up to 8440 bytes) with 16-bit CRCs for error detection, with either Hamming code or Reed Solomon (RS) coding for error correction.

8.1 Modulation

The 4-FSK scheme running at 4.8 ksymbols/s (9.6 kbps) can be used to fit inside a 12.5kHz channel bandwidth, a rate of 9.6 ksymbols/s (19.2 kbps) can be used in 25kHz bandwidth channels. Channel bandwidth is dependent on the peak deviation that the modulating signal causes the carrier to deviate by as well as the data rate.

The bit to symbol mappings that this Function Image™ uses for 4-FSK with a RRC alpha 0.2 plus sinc filter are:

4-FSK bit to symbol mapping		Deviation (Hz)	
Input Bit Pair	Relative Symbol Level	12.5kHz channel	25kHz channel
00	-1	-800	-1600
01	-3	-2400	-4800
10	+1	+800	+1600
11	+3	+2400	+4800

Table 2 Mapping and Deviation

When transmitting the preamble sequence, this results in a sine wave signal with a peak deviation of either +/- 3.056kHz or 6.108kHz for 4.8 and 9.6 ksymbols/s respectively.

8.2 Radio Interface

The transmit radio interface can be set to two-point modulation or I/Q. When the device is in two-point modulation mode the I Output is used as ‘Mod 1’, and the Q Output is used as ‘Mod 2’. The receive signal must come from an I/Q radio receiver.

8.2.1 I/Q Transmit and I/Q Receive Interfaces

The device can produce an I/Q modulated signal, taking a baseband modulating signal and using it to frequency modulate an I/Q baseband signal, with a user programmable deviation.

In receive the device will accept an I/Q input signal and provide significant channel filtering digitally. It will then frequency demodulate the resulting signal, which is treated as a limiter discriminator output signal would be internally. An overview of how the CMX7364 might use the CMX994E[3] for reception and the CMX998[4] for transmission is shown in Figure 30. The internal functions of the CMX7364 when operating

[3] CMX994E is a Direct Conversion Receiver

[4] CMX998 is a Cartesian Feedback Loop Transmitter which is designed primarily for non-constant envelope modulations such as QAM although it will also support GMSK/4-FSK; conventional I/Q vector modulators such as the CMX993 would be more typical of solutions for GMSK/4-FSK modulation.

in this mode are shown in Figure 2. An alternative solution would be to use the CMX992 instead of the CMX994, this FI allows operation with either receiver solution.

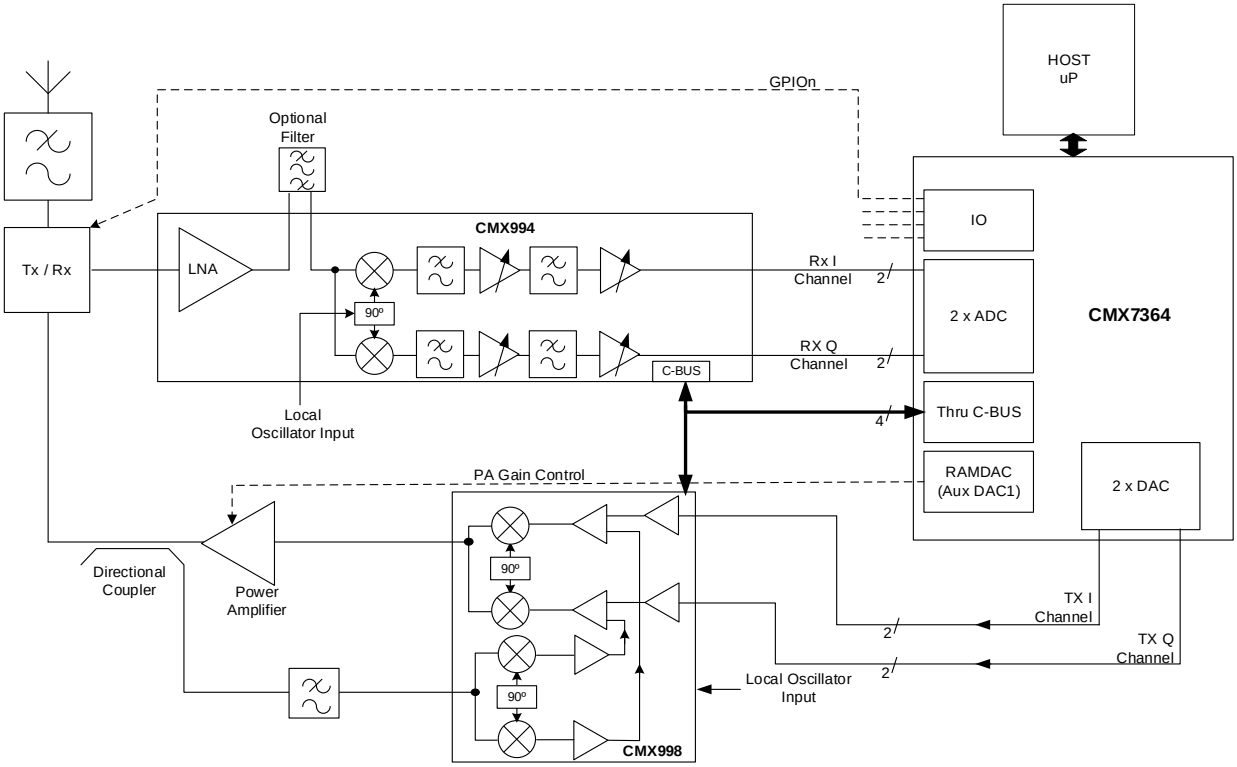


Figure 30 Outline Radio Design (I/Q in/out)

Use of I/Q receive mode results in dc offsets caused by the radio receiver – resulting in the signal into the CMX7364 having a dc offset other than BIAS. This offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7364.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7364. However the CMX7364 does provide dc offset calculation and removal. These are described in detail in the application note section 11.2 DC Offsets in I/Q Receivers.

8.2.2 Two-point Modulation Transmit with I/Q Receive Interface

An overview of how the CMX7364 might integrate with an I/Q receiver, and two-point modulation transmitter is shown in Figure 31. The internal functions of the CMX7364 when operating in this mode are shown in Figure 3.

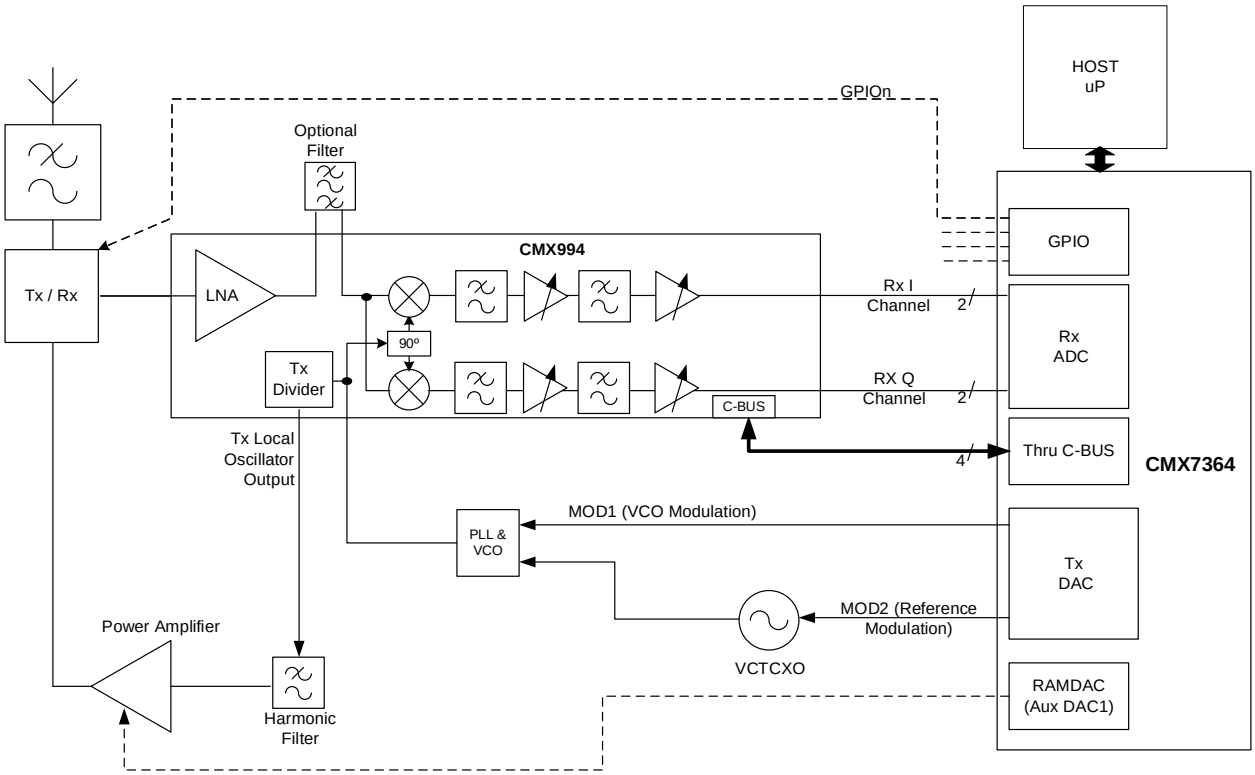


Figure 31 Outline Radio Design (4-FSK – I/Q in, two-point mod out)

8.3 RTCM SC135 Formatted Data

When transmitting/receiving 4-FSK the 7364FI-8.x supports RTCM SC135 style of formatted data which provides the ability to encode blocks of data using Hamming codes, RS codes and CRCs. Please refer to the SC135 standard document from the RTCM website for further information.

RTCM SC135 Frame Type 0 (without FEC) and Frame Type 1 (with FEC) are supported. The Function Image™ will automatically insert Preamble, Frame Sync pattern, Frame Type symbols, CRCs and will add the appropriate FEC schemes to the header and data payloads for each frame type.

In Tx mode, the Frame Type is selected by writing the appropriate command to the Modem Command FIFO Control Byte - $4A write register: see section 10.1.3. The data can then be written to the Modem Command FIFO Data Byte - $48 write register.

The first 5 bytes to be written are bytes 1 to 5 of the RTCM SC135 header. See Section 6.1 of the standard. These 5 bytes are then followed by any optional header data and payload data bytes. The CRCs will be inserted automatically by the Function Image™.

The header length value written in byte 3 should be 5 + length of the Optional Packet Header.

For example: assuming that 12 bytes of optional header data and 64 bytes of payload data are to be sent, the host would write 0x87, 0x00, 0x11, 0xE0, 0x40, followed by the 12 optional header data byes and the 64 payload data bytes to the Command FIFO Data Byte - $48 write register. The Function Image™ will automatically increment the Header Length field to include the 8 bit CRC which is automatically inserted and it will insert the sequence number into header byte 2.

The Function Image™ will partition the following payload data into code-blocks, appending 16 bit CRCs and any necessary parity bytes to each code-block.

In Rx Mode, once a frame sync pattern has been detected, the frame type and length of data will be automatically detected by the Function Image™. The frame type received will be indicated by the control byte. See section 10.1.26.

RTCM SC135 frames consist of a header packet followed by a variable length data payload which will be separated into one of more code blocks each of which may be of different lengths. The Function Image™ will first write the control byte and then 5 data bytes of the RTCM SC135 header in to the Receive FIFO. For each code block that follows, the control byte will be updated to indicate whether or not a CRC error has occurred for that code block. The next data byte will indicate the number of code blocks to follow and the code block number. The next 2 bytes should be used to form a 16 bit number indicating the number of data bytes to follow. Then the Function Image™ will write the *n* data bytes of the code block into the Receive FIFO. This process will repeat until all *N* received code blocks have been written to the Receive FIFO. See Figure 32 Received RTCM SC135 Frame.

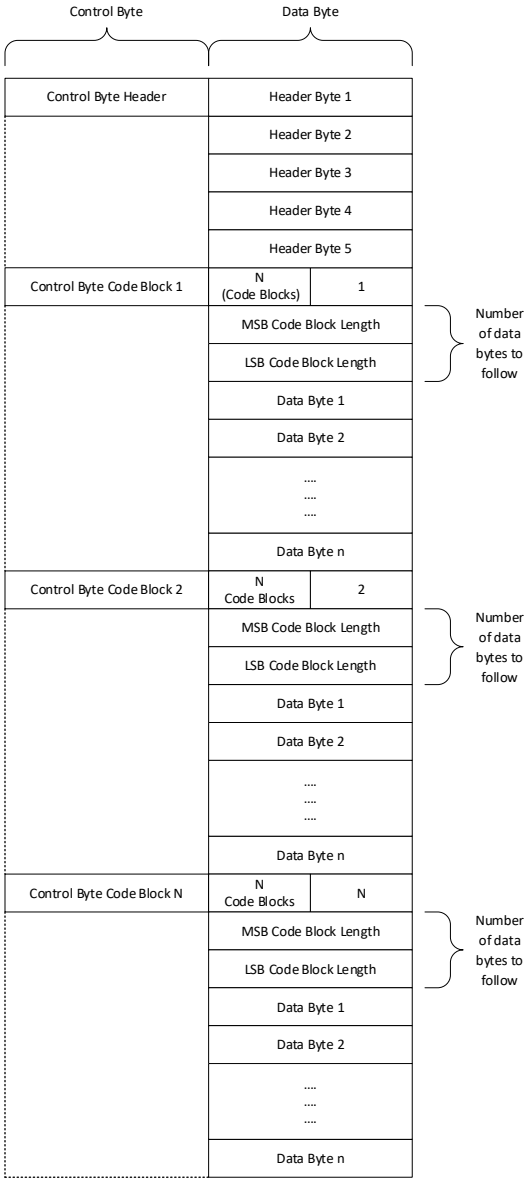


Figure 32 Received RTCM SC135 Frame

8.4 Receiver Response Equaliser

When receiving signals using a radio receiver the signal provided to the CMX7364 is likely to be distorted. Considering the architecture of Figure 30 as typical, the distortion will largely be caused by the crystal filter – shown as a bandpass filter in the diagram. The crystal filter operates on the received signal at an intermediate frequency; its purpose is to attenuate unwanted signals such as those on adjacent channels before they get to the CMX7364.[5]

Typically the pass band of the crystal filter is not flat or perfectly linear phase, resulting in the wanted signal being distorted due to the amplitude/phase response of the filter. The result is usually a degraded receive signal which will result in a small degradation in 4-FSK reception.

Other radio architectures may provide baseband filtering in order to help reject unwanted adjacent channel signals. Such filtering may also have a pass band that is not flat, and therefore will degrade reception in a similar way.

The CMX7364 provides a Receiver Response Equaliser that will compensate for the group delay and variation in gain of the crystal filter, or any other distortions present in the received signal. The equaliser must be trained with a clean, high level, 4-FSK signal in order to establish the receiver response and produce a filter which compensates for it. Once this filter is calculated it may be read from the CMX7364 and stored for later use. The CMX7364 can be configured with up to two previously stored Receiver Response Equaliser filters which may, for example, be used to compensate for two different crystal filters in a radio designed to receive in two channel bandwidths.

A suitable training signal may either be produced using another CMX7364 or a signal generator using preamble, frame sync and pseudo-random data, along with pulse shaping filters that are compatible with the FI-8.x signal specification within this datasheet.

The Receiver Response Equaliser has two modes, single mode produces better results when correcting for receivers with a simple baseband roll off (for example in a direct conversion architecture). Dual mode produces better results when compensating for a radio receiver which includes a crystal filter. Program Block 11 – Receiver Response Equaliser provides equaliser mode selection, allows adjustment of the gain used in the feedback path when training the equaliser and allows the training time to be altered. The same Program Block allows the filter resulting from training to be read for storage and to be programmed back in to the CMX7364 later for use when receiving.

Results when using the Receiver Response Equaliser are shown in section 8.6.3 Receiver Response Equaliser Performance.

See:

- 10.1.19 Modem Mode and Control - $6B write
- 10.2.13 Program Block 11 – Receiver Response Equaliser

8.5 Typical Transmit Performance

Using the test system shown in Figure 33 the 7364FI-8.x internal PRBS generator can be used to modulate an RF vector signal generator.

[5] Note that the CMX7364 provides significant channel filtering itself, but further rejection of unwanted signals is desirable in most applications to improve receiver dynamic range and prevent blocking or products generating intermodulation products reaching the low power ‘back-end’ of the receiver.

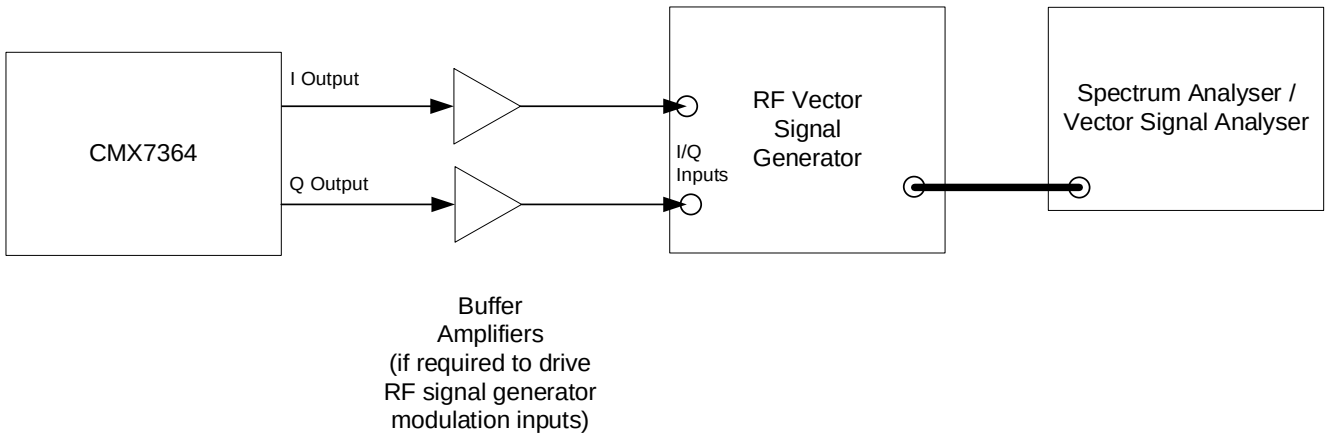


Figure 33 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

8.5.1 Tx Spectrum Using DE9941A

The following figures were produced using the DE9941A as the transmit and receive hardware, which is representative of a real-world implementation using I/Q transmit and receive. The desired deviation was achieved by adjusting the CMX7364 peak deviation using register $61. For the Modulation Spectrum shown in Figure 34 and Figure 37, the following conditions apply (performance is specified against limits in the EN 300 113 standard):

	12.5 kHz Channel	25 kHz Channel
Measurement Bandwidth	8.5 kHz	18 kHz
Symbol Rate	4.8 ks/s	9.6 ks/s
Tx Filter	RRC – 0.2 + Sinc	RRC – 0.2 + Sinc
Peak Deviation (+3 symbols)	2.4 kHz	4.8 kHz
Pre-amble Peak Deviation (RTCM SC135)	3.056 kHz	6.108 kHz
1st ACP	< 65 dBc (limit -60 dBc)	< 65 dBc (limit -60 dBc)
2nd ACP	< 65 dBc (limit -60 dBc)	< 65 dBc (limit -60 dBc)

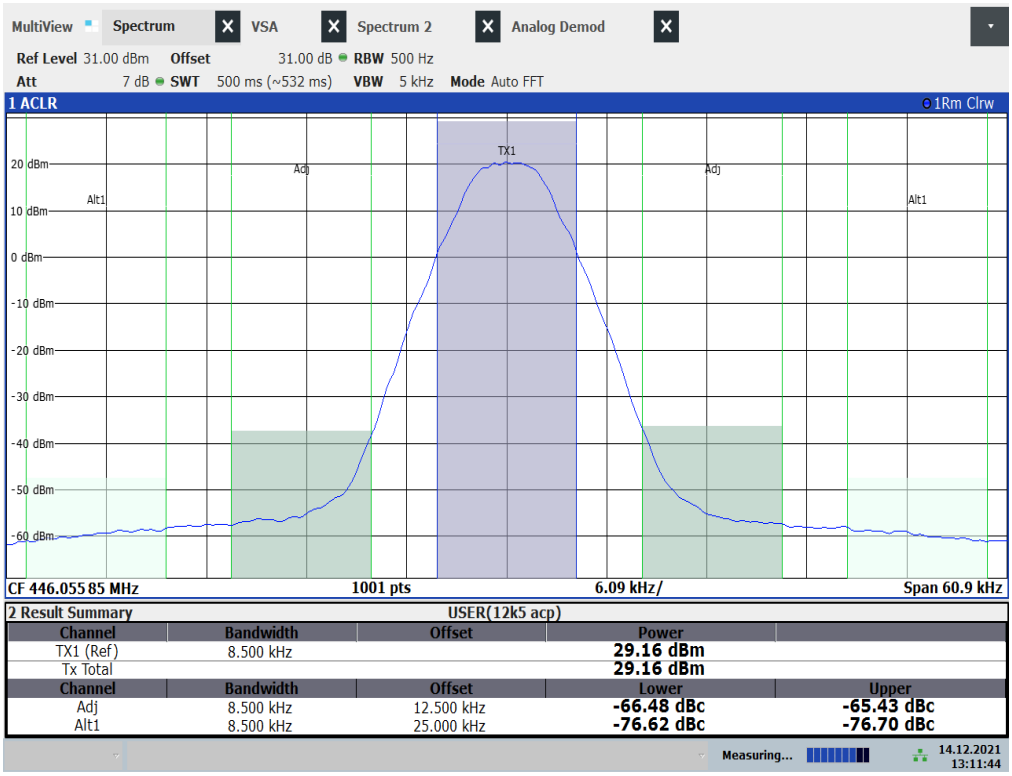


Figure 34 Tx Adjacent Channel Power for 12.5kHz I/Q Mode

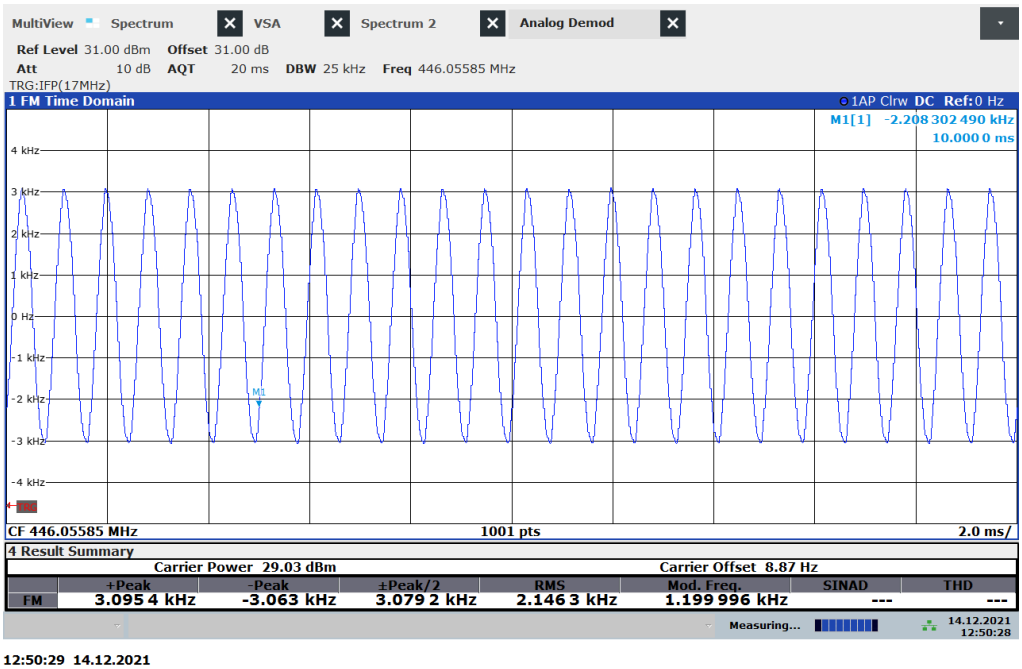


Figure 35 Preamble Pattern for 12.5kHz I/Q Mode

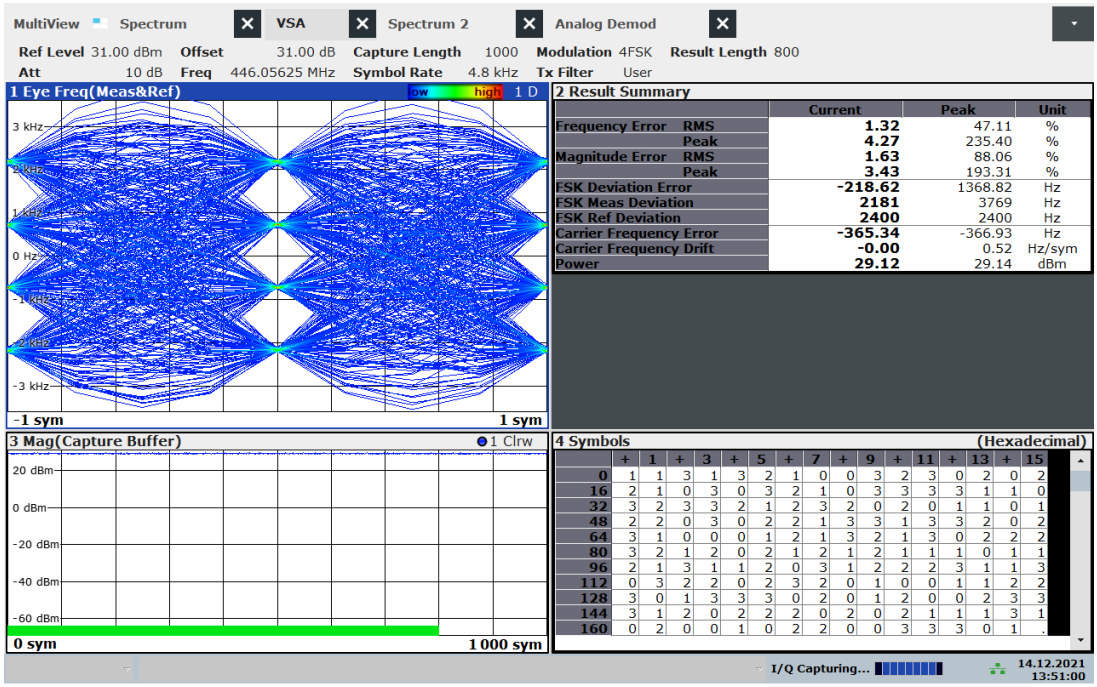


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Figure 36 Eye Pattern for 12.5kHz I/Q Mode

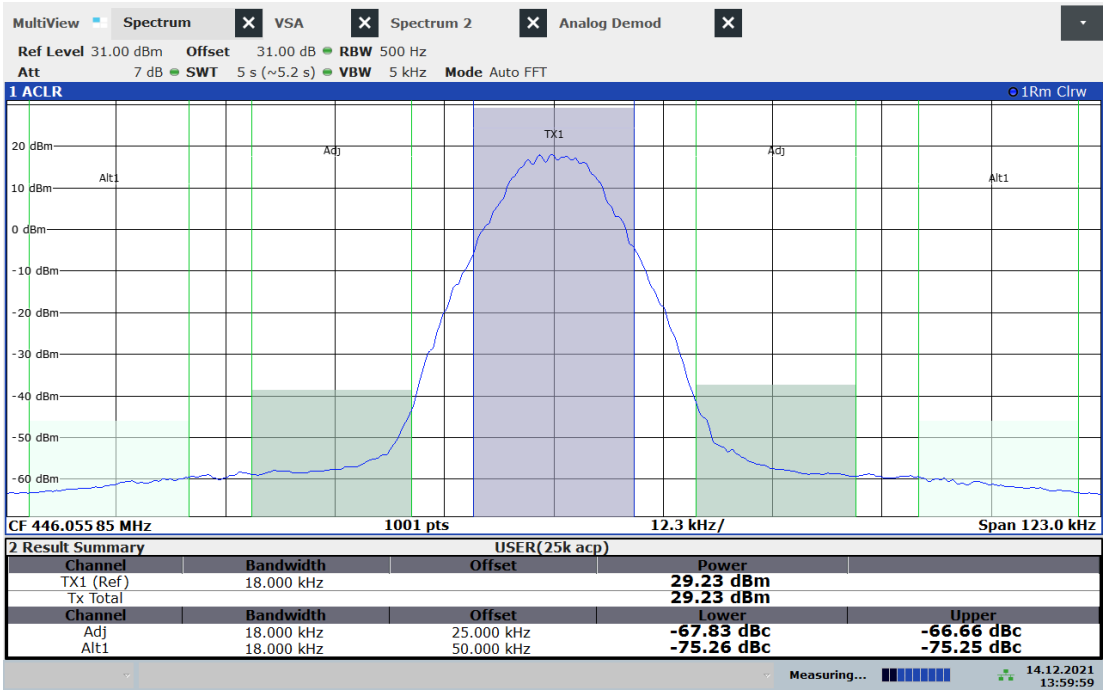

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Figure 37 Adjacent Channel Power for 25kHz I/Q Mode

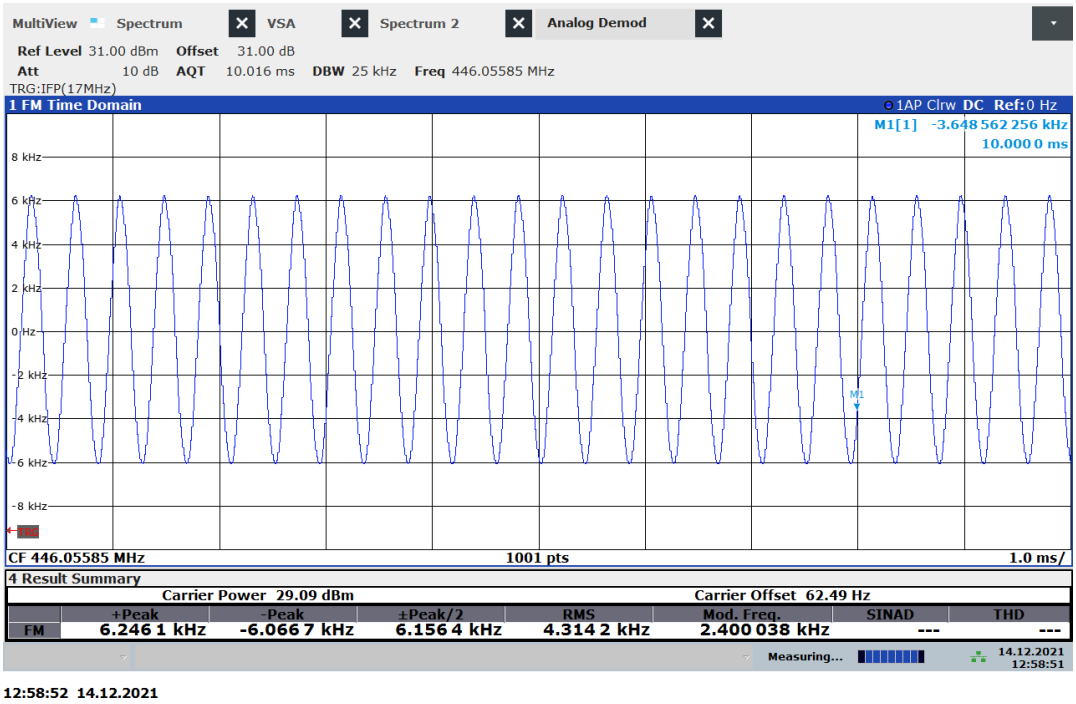


Figure 38 Preamble Pattern for 25kHz I/Q Mode

8.5.2 Tx Spectrum using two-point modulation

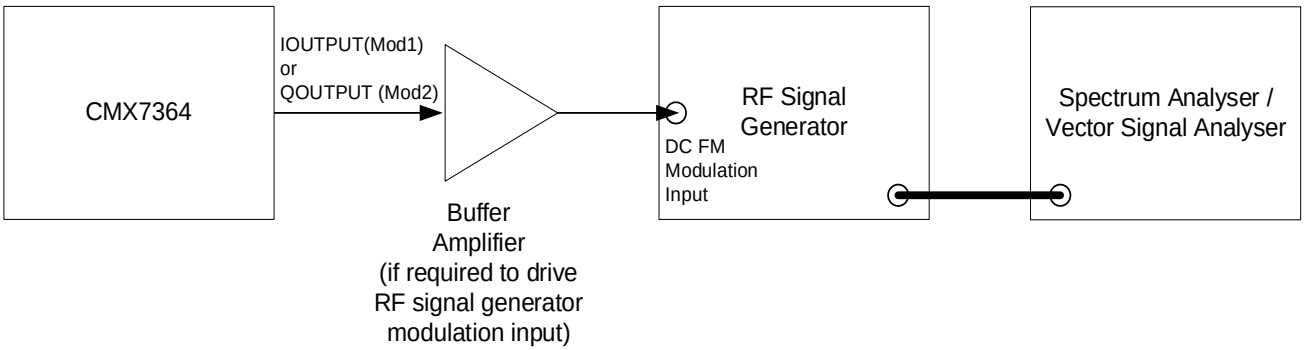


Figure 39 Tx Spectrum and Modulation Measurement Configuration for Two-point Modulation

Using the test system shown in Figure 39 the internal PRBS generator was used to modulate the RF FM signal generator. Some typical results are shown in the following figures. The desired deviation was achieved by adjusting the deviation control in the RF signal generator. For the Modulation Spectrum shown in Figure 40, the following conditions apply:

- EN 300 113 Adjacent Channel measurement for 25kHz channel:
- ACP < -65dB (limit is –60dB)
- Integration window = 16kHz

- Peak deviation (+3 symbol) = 4.8kHz

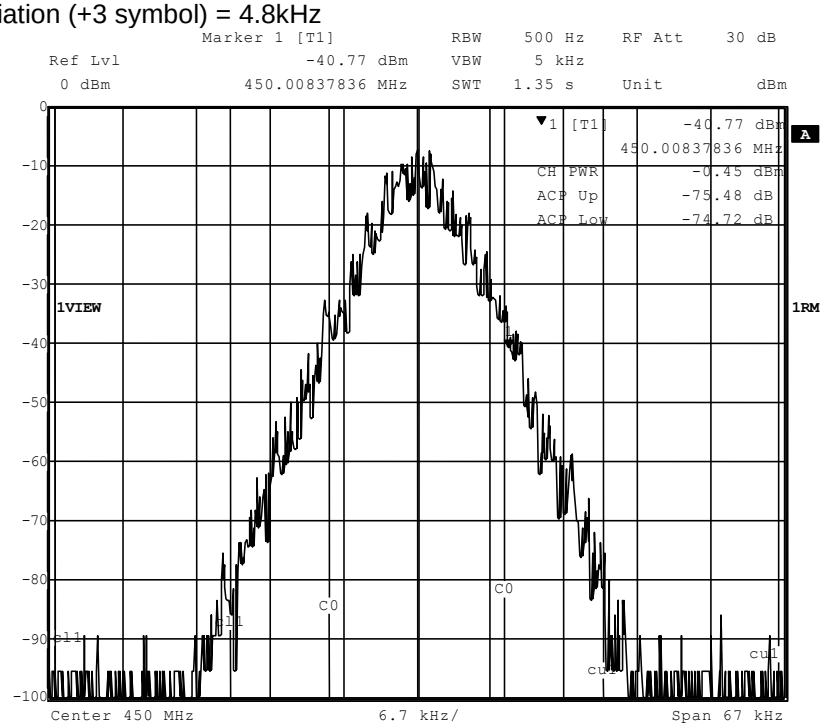


Figure 40 Modulation Spectrum, 25kHz Two-point Mode

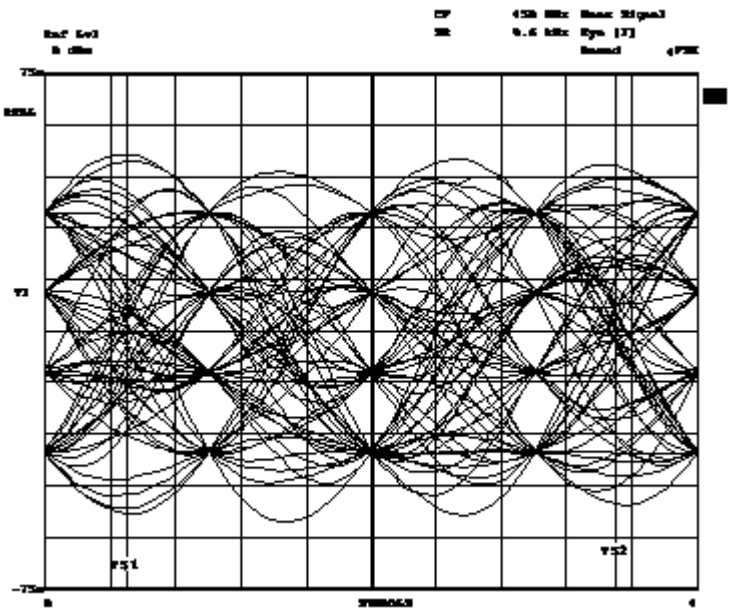


Figure 41 Tx Eye Diagram, 25kHz Two-point Mode

8.6 Typical Receive Performance

This is provided to serve as guidance, however, each user must consider his own application requirements and then select both the receiver used and any coding (whether used and if so block size and code rate, where applicable).

8.6.1 4-FSK

8.6.1.1 Signal-to-Noise and Co-channel Performance

The performance of the device when receiving is shown in the following graphs. Data is provided showing a selection of representative cases ranging from best case performance (with FEC) to worst case where no coding is used (raw mode) plus the effect of using the two supported types of data pulse shaping: plain Root Raised Cosine (RRC) filtering or RRC plus sinc filter.

In the following graphs, the modulation is 4-FSK and the data rate is dependent on channel bandwidth. The 25kHz channel data rate is 9.6ksymbols/s, the 12.5kHz channel data rate is 4.8ksymbols. The signal-to-noise ratio is calculated as:

SNR = Mean signal power – (-174 dBm + NF +10 log10(RxBW))

Where:

NF = receiver noise figure in dB
RxBW = receiver noise bandwidth in Hz
Mean signal power in dBm
SNR = Signal-to-Noise Ratio in dB.
Thermal noise power (in a 1 Hz bandwidth) is approximately -174 dBm

The graph in Figure 42 compares the raw sensitivity performance of data transfer using a 12.5kHz and a 25kHz channel, in each case the deviation of the transmitted modulation has been adjusted to give a realistic Tx ACP, in the 12.5kHz case the Tx ACP was ~63dBc and in the 25kHz case the Tx ACP was ~73dBc. The pulse shaping filter used was an RRC with no sinc filter in place. The modulation parameters used in all of the figures that follow in this section are summarised below. Note that RTCM SC135 operation assumes the use of Sinc filter to achieve the specified deviation whilst remaining within the channel boundaries.

Channel Bandwidth (kHz)	Baud Rate (Symbols/s)	Pulse Shaping Filter	Deviation (kHz)	Measured Tx ACP (dBc)	Receiver Noise Bandwidth (kHz)	Used in Figures
25	9600	RRC Only	2.85	72	18	Figure 42
12.5	4800	RRC + Sinc	2.4	63	9	Figure 43
12.5	4800	RRC Only	1.9	63	9	Figure 42

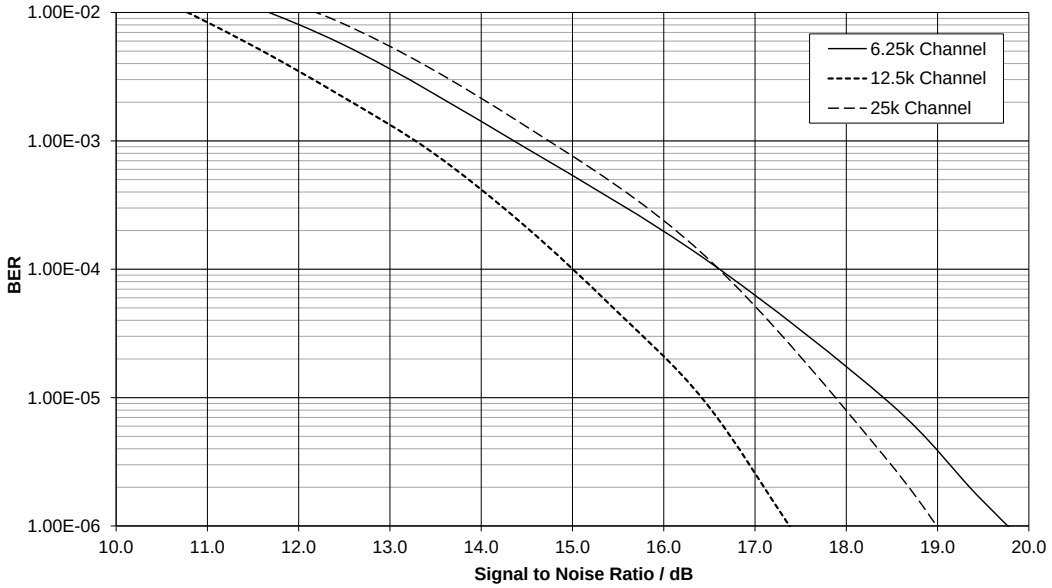


Figure 42 Modem Sensitivity Performance (Root Raised Cosine Pulse Shaping)

The 7364FI-8.x supports pulse shaping filters using an RRC plus sinc filter option (as specified in RTCM SC135). Simply switching from a RRC Only filter to this filter reduces the bandwidth of the modulated signal – so an increased deviation can be used. The graph in Figure 43 compares the performance of a 12.5kHz channel system with and without the sinc filtering included. It can be seen that the sinc filter degrades the sensitivity by less than 0.5dB when there is no change in the deviation level.

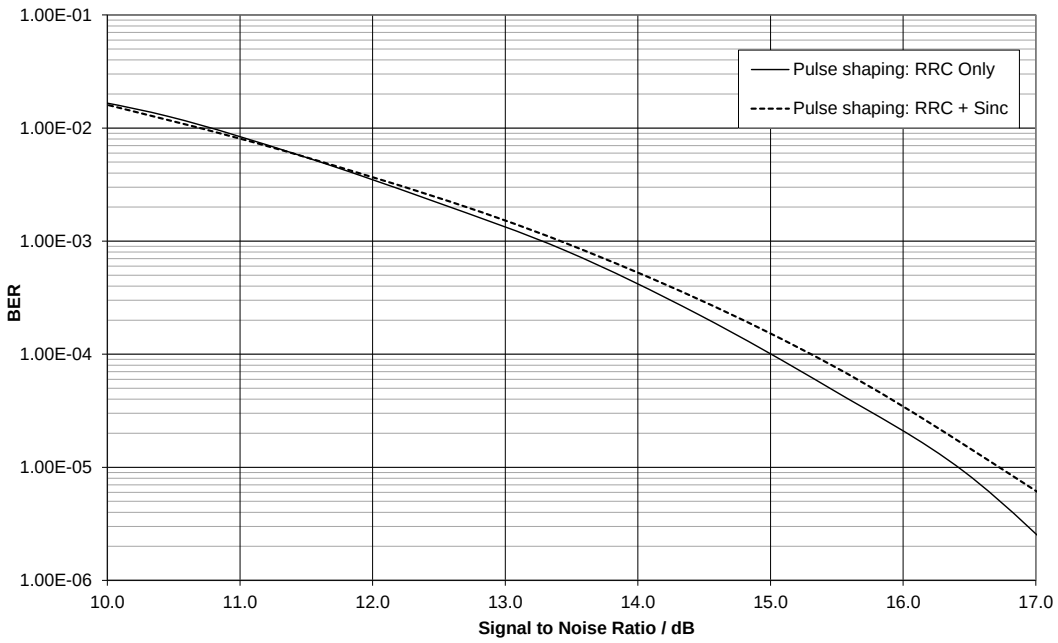


Figure 43 12.5kHz Channel Sensitivity With and Without Sinc Filter Comparison

The RTCM standard specifies that no data should be decoded if the Header packet is received in error. Figure 44 shows the Packet Error Rate for the Header packet for both Type 0 (No FEC) and Type 1 frame types in a 12.5kHz channel at 4.8ksymbols/s (with an RRC + sinc pulse shaping filter) when using the DE9941A.

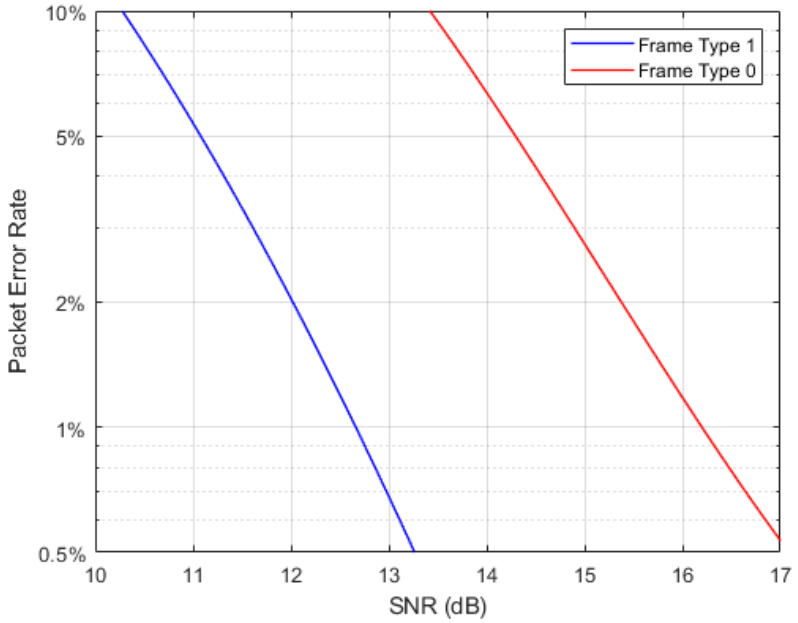


Figure 44 RTCM Header Packet Error Rate: 12.5kHz Channel, 4.8ksymbols/s

The co-channel rejection ratio (Figure 45) is measured with an interferer modulated with 400Hz FM and having a deviation of 1.5kHz; which is 12% of the nominal 12.5kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests.

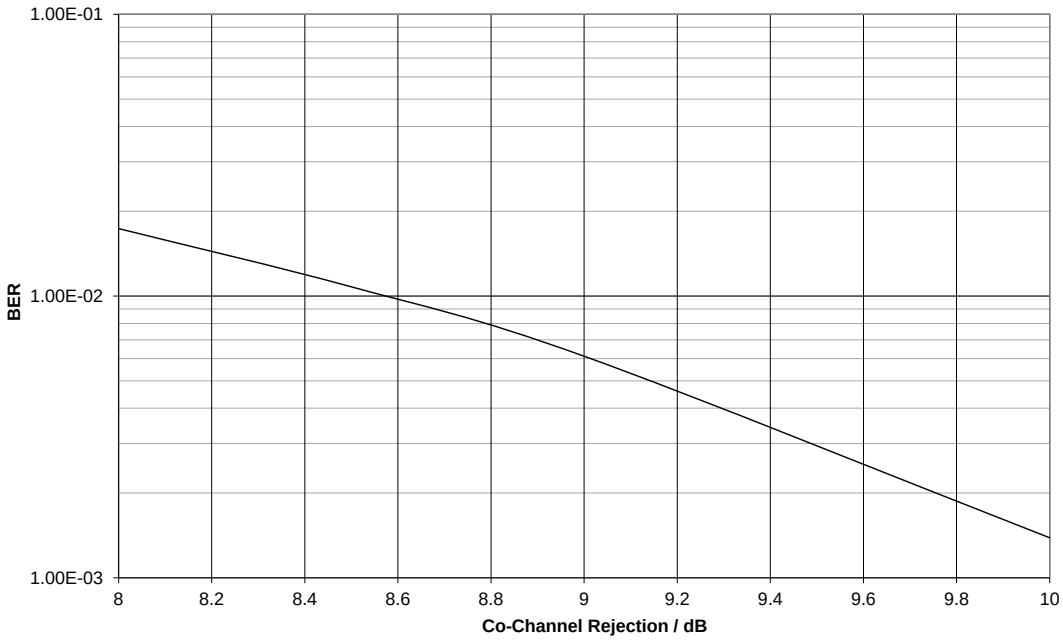


Figure 45 Modem Co-channel Rejection with FM Interferer (as EN 300 113)

8.6.1.2 Adjacent Channel Performance

The 7364 FI-8.x provides excellent rejection of adjacent signals present on the I/Q inputs. Assessment of the adjacent channel rejection (ACR) performance of the modem is normally made in terms of BER or PER for a given ratio between the wanted signal (on channel) and larger interferer on the adjacent channel. Detailed measurement methods vary depending on the standards in use, in particular whether the wanted signal is raised above the sensitivity limit and where the reference is taken. The figures quoted here are based on the measurement method from EN 300 113. The BER curve shown in Figure 46 is based on the difference between the interferer (400Hz FM modulation, 1.5kHz deviation) and the power of the wanted signal for 4.8ksymbols/s.

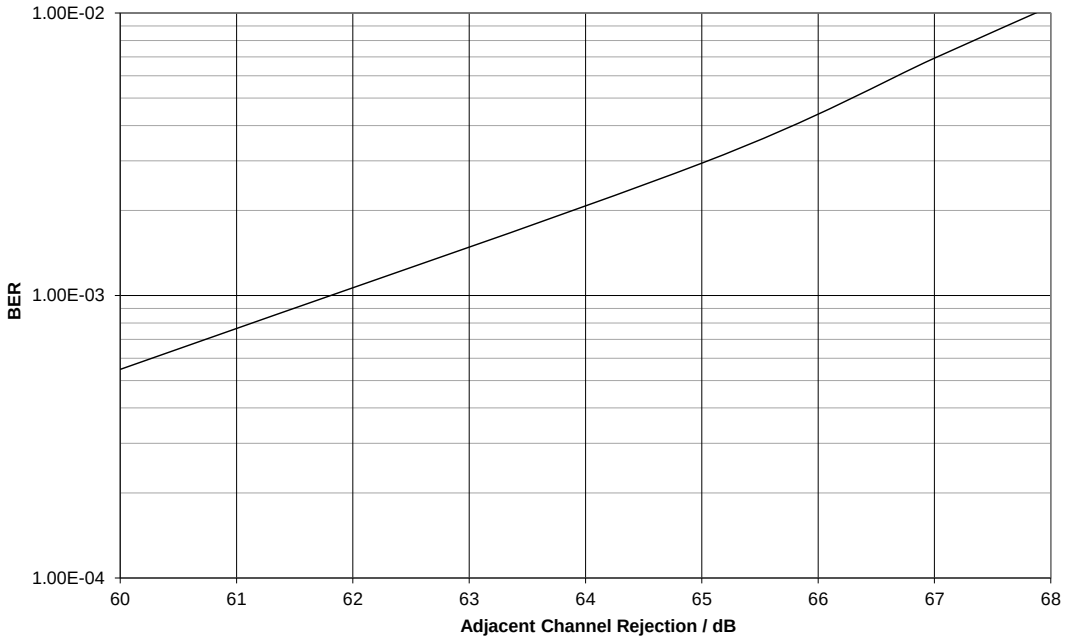


Figure 46 ACR Rejection Performance

The results in Figure 46 are typical of what may be achieved with 7364FI-8.x and a typical I/Q radio receiver with no adjacent channel selectivity in the radio circuits. In a more normal RF architecture, some adjacent channel selectivity will be provided making system results better than the measured values for the 7364FI-8.x alone. Furthermore, the results observed are not necessarily the maximum that the CMX7364 can achieve but are limited by the practical dynamic range of the CMX7364 combined with the system gain and noise figure of the receiver used in these tests.

8.6.2 Receiver Dynamic Range

The adjacent channel rejection results in section 8.6.1.2 also indicate that a wanted signal can be successfully received over the dynamic range shown in Figure 46 without any need for an AGC. Note that this is limited at the top end by the maximum allowed signal amplitude into the CMX7364, but performance at the bottom end is affected by noise added by the test receiver – so these figures are not the absolute limit of CMX7364 performance.

8.6.3 Receiver Response Equaliser Performance

The performance of the 7364FI-8.x when receiving a signal using the EV9942 (CMX994/A/E with temperature compensated baseband filter) is shown in the following graphs. The EV9942 includes a baseband channel filter, the nominal bandwidth of which is 8kHz (-3dB)[6].

The following tests were carried out using a 4.8ksymbols/s, 8-FSK or 16-FSK signal and are representative for a typical 12.5kHz RF channel. Where the results are quoted as using no equalisation the Receiver Response Equaliser was disabled. Where the results are quoted as Equalised the Receiver Response Equaliser was provided with a training sequence at a level of –70dBm, which produced 400mV (differential) on the I and Q inputs. Equaliser gain was set to 1000 and training lasted for 10000 symbol periods. While training, the received signal had less than 100Hz frequency error. Once trained, the resulting equaliser coefficients were used for the remaining tests.

Firstly the signal-to-noise performance of equalised and non-equalised received signals are compared. The test is similar to that described in 8.6.1.1 Signal-to-Noise and Co-channel Performance.

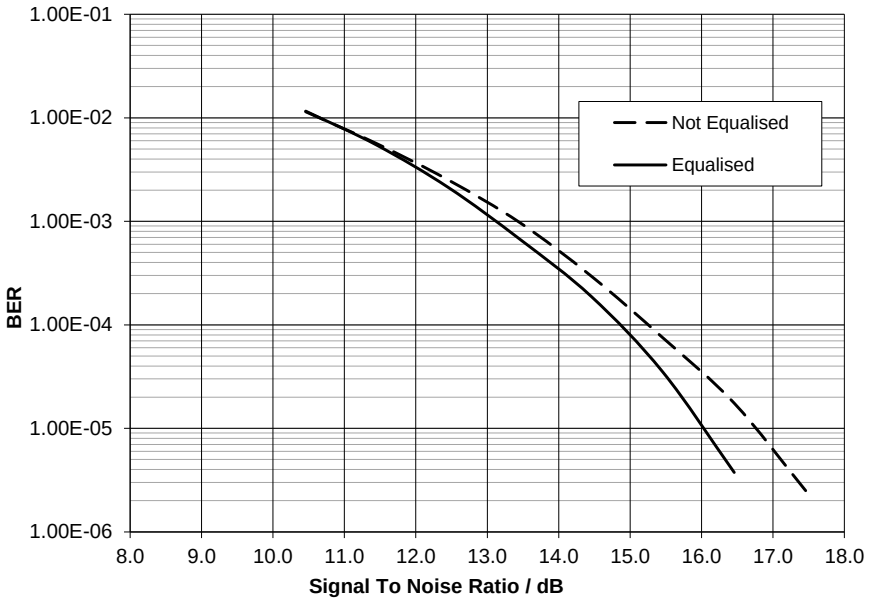


Figure 47 4-FSK Signal-to-Noise Performance, Equalised and Non-Equalised

[6] EV9942 with default components fitted and 'Mid' channel bandwidth selected Rx Control Register ($12), b4-b3 = '01'.

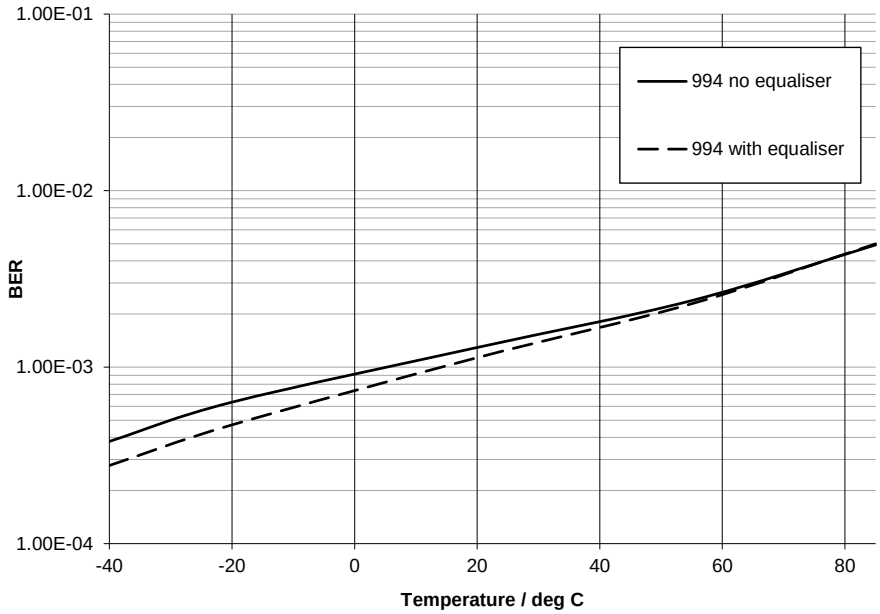


Figure 48 Performance of Equalised Signals with Temperature Variation

Tests were carried out using modulation with a signal to noise ratio of 13dB using the EV9942 (CMX994/A/E with temperature compensated baseband filter). BER performance was measured with and without equalisation being applied then the temperature was varied and the equalised and non-equalised bit error rate measurements repeated. The results are shown in Figure 48. The results show that equaliser performance is maintained across the full operating temperature range. For all results the frequency error between transmitter and receiver was less than 100Hz.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

Q1 Package (64-pin VQFN)	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25ºC		3500	mW
Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
Voltage differential between power supplies:				
DV_{DD} and AV_{DD}	0	–	0.3	V
DV_{SS} and AV_{SS}	0	–	50	mV
Operating Temperature	-40	–	+85	°C
Xtal Frequency	3.0	–	12.288	MHz
External Clock Frequency	3.0	–	25.000	MHz

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz±0.002% (20ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.

Current consumption figures quoted in this section apply to the device when loaded with FI-8.x only. Current consumption may vary with other valid Function Images™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current (see also section 9.1.4)	11				
All Powersaved					
AI_{DD} + DI_{DD}	10,15	–	120	–	µA
Idle Mode	12,15				
DI_{DD}	13	–	550	–	µA
AI_{DD}		–	17	–	µA
Additional Current for One Auxiliary System Clock (output running at 5MHz – SYSCLKPLL active)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	900	–	µA
Additional Current for one Auxiliary System Clock (output running at 4.8MHz – SYSCLKPLL not required)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	675	–	µA
Additional Current for Each Auxiliary ADC	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	190	–	µA
Additional Current for Each Auxiliary DAC	14,15				
AI_{DD} (AV_{DD} = 3.3V)		–	210 to 370	–	µA

Notes:
10 Idle mode with V_{BIAS} disabled.
11 T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
12 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled and V_{BIAS} enabled.
13 Using a 19.2MHz external clock input, Xtal oscillator circuit powered down.
14 A lower current is measured when outputting the smallest possible dc level from an AuxDAC, a higher current is measured when outputting the largest possible dc value.
15 Using a 19.2MHz external clock input.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	11	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	11	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes: 20 Characteristics when driving the XTAL/CLK pin with an external clock source.

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor, as shown in section 4.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
SYSPLL Operating Frequency			38	–	250	MHz
SYSCLK1/2 Output Frequency			–	–	20	MHz
Rise Time			–	–	13.5	ns
Fall Time			–	–	6	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Differential I and Q Inputs						
Input Impedance, Enabled		31	10	–	140	kΩ
Input Impedance, Muted or Powersaved				200		kΩ
Maximum Input Voltage Excursion		32	–	–	20 to 80	%AV_{DD}
Programmable Input Gain Stage						
Gain (at 0dB)		33	−0.5	0	+0.5	dB
Cumulative Gain Error (w.r.t. attenuation at 0dB)		33	−1.0	0	+1.0	dB

Notes:

30 Timing for an external input to the XTAL/CLOCK pin.

31 With no external components connected.

32 For each input pin and for AV_{DD} = 3.3V, the maximum allowed signal swing is: (3.3 x 0.8) - (3.3 x 0.2) = 2.0V.

33 Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
Modulator I/Q Outputs (I Output, Q Output)						
Power-up to Output Stable		40	–	50	100	µs
I/Q Output Coarse Gain Attenuators						
Attenuation (at 0dB)		42	−0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		42	−0.6	0	+0.6	dB
Output Impedance	Enabled	41	–	600	–	Ω
	Disabled	41	–	>100	–	MΩ
Output Voltage Range		43, 44	0.3	–	AV_{DD}-0.3	V
Load Resistance			20	–	–	kΩ

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

42 Figures relate to attenuator block only. Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

43 For each output pin. With respect to the output driving a 20kΩ load to $AV_{DD}/2$.

44 The levels of I/Q Output Fine Gain and Offset (registers $5D and $5E) should be adjusted so that the output voltage remains between 20% and 80% of AV_{DD} on each output pin (when 0dB of coarse output gain is used). This will produce the best performance when the device operates with AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AuxADC1-4)					
Source Output Impedance	50	–	–	24	kΩ
Auxiliary 10-Bit ADCs					
Resolution		–	10	–	Bits
Conversion Time	51	–	225	–	µs
Sample Rate		1	-	512	Hz
Input Impedance					
Resistance	56	–	26.5	30	kΩ
Capacitance	56	–	3	3.5	pF
Offset Error	54, 55	–	–	±18	mV
Integral Non-linearity	54, 55	–	–	±2	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Conversion Time	51		60		µs
Settling Time to 0.5 LSB			10		µs
Offset Error	54, 55	–	–	±20	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	54, 55	–	–	±4	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs

Notes:

50 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

51 Typical – based on 9.6MHz Xtal or external oscillator

52 Guaranteed monotonic with no missing codes.

54 Specified between 2.5% and 97.5% of the full-scale range.

55 Calculated from the line of best fit of all the measured codes.

56 The input signal internally drives a S/H (sample and hold) circuit that is newly charged for one ADC conversion period on each ADC conversion. That circuit connects the input pin to an internal $V_{DD}/2$ voltage source via a series resistor-capacitor network. The S/H circuit's net time constant, including the external source impedance of any input signal, will determine the S/H settling time. Provided the external source impedance is of low value, the resultant settling time will be correspondingly small. Using the above figures and calculating time t = 9 time constants x R x C, the result would be 9 * 30kΩ * 3.5pF = 0.95µs.

9.1.4 7364FI-8.x Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in section 5.
Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz ±0.002% (20ppm) clock input; T_{AMB} = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Signal-to-Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-8.x only. The use of other valid Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (4.8ksymbols/s – search for FS)		–	10.9	–	mA
DI_{DD} (9.6ksymbols/s – search for FS)		–	20	–	mA
		–		–	
DI_{DD} (4.8ksymbols/s – FS found)		–	6.3	–	mA
DI_{DD} (9.6ksymbols/s – FS found)		–	11	–	mA
		-		-	
AI_{DD} (AV_{DD} = 3.3V)		–	6.6	–	mA
Tx Mode	69				
DI_{DD} (4.8ksymbols/s)		–	5.9	–	mA
DI_{DD} (9.6ksymbols/s)		–	10.1	–	mA
		-		-	
AI_{DD} (AV_{DD} = 3.3V)		–	8.4	–	mA

Notes:

69 Transmitting in I/Q mode, continuous 4-FSK PRBS, all GPIOs and RAMDAC set to manual.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		4800		9600	sym s^{-1}
Modulation			4-FSK		
Filter RRC Alpha			0.2		
Tx Bit-rate Accuracy	70		-		ppm
Tx Output Level (I Output, Q Output)	71				
FI-8.x I/Q modulation mode			2.6		Vp-p
FI-8.x Two-point modulation mode			4.1		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	72	-	-	-	dB
Rx Frequency Error Tolerated	75		+/- 1.0		kHz
Rx Co-channel Rejection	73	-	-	-	dB
Rx Adjacent Channel Rejection	73	-	-	-	dB

Notes:

70 Determined by the accuracy of the Xtal oscillator provided.

71 Transmitting continuous PRBS data. This is a differential voltage;
I Output = IOUTPUTP-IOUTPUTN and Q Output = IOUTPUTP-IOUTPUTN.

72 See section 8.5 Typical Transmit Performance

73 See section 8.6 Typical Receive Performance

75 Optimum performance is achieved with 0Hz frequency error. The figure quoted is for a symbol rate of 9.6ksymbols/s. The frequency error tolerated is proportional to the symbol rate.

9.2 C-BUS Timing

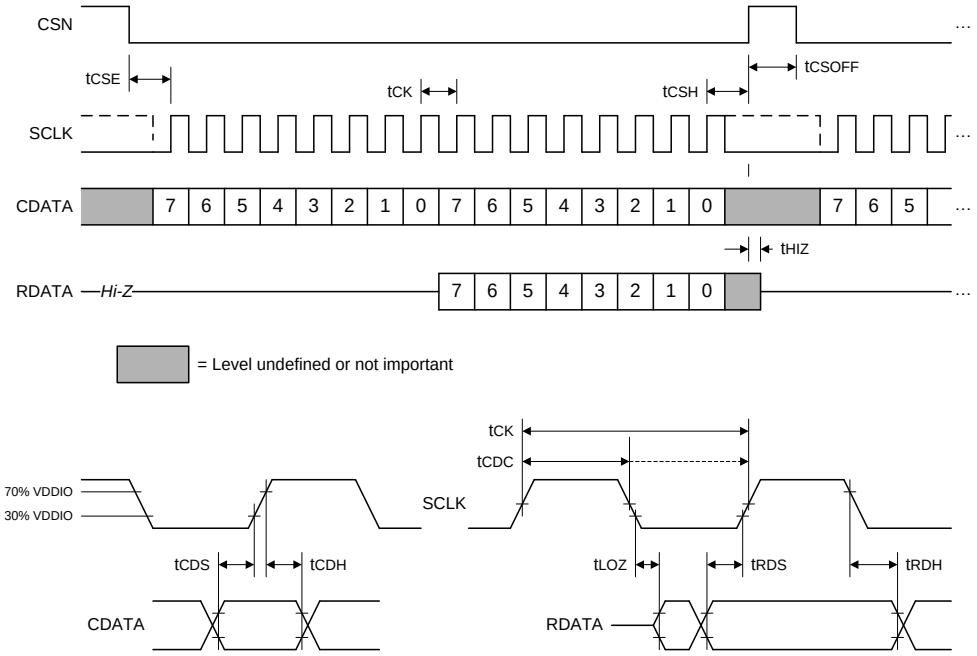


Figure 49 C-BUS Timing

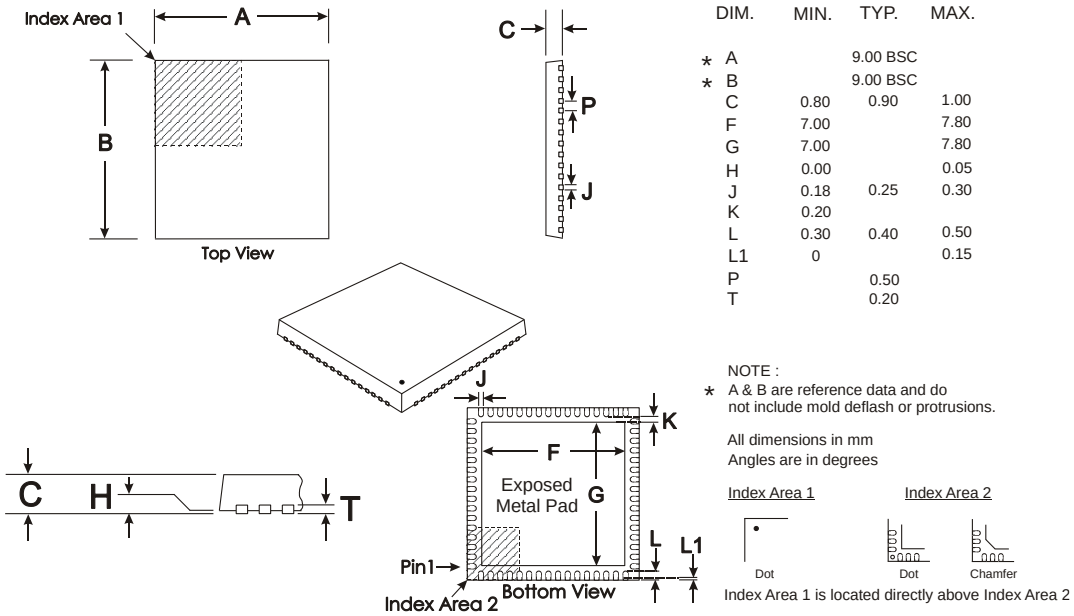
AC Parameters	Notes	Min.	Typ.	Max.	Unit
C-BUS Timing	1, 2				
Input pin rise/fall time (10% - 90% of VDDIO)		–	–	3	ns
Capacitive load on RDATA and IRQN		–	–	30	pF
t_{CSE} CSN enable to SCLK high time		40	–	–	ns
t_{CSH} Last SCLK high to CSN high time		40	–	–	ns
t_{LOZ} SCLK low to RDATA output enable time		0	–	–	ns
t_{HIZ} CSN high to RDATA high impedance		–	–	40	ns
$t_{CSOFF(wr)}$ CSN high time for Write transactions and FIFO Reads		50	–	–	ns
$t_{CSOFF(rd)}$ CSN high time for Read transactions (except FIFO)	3	50 / 2000	–	–	ns
t_{CDC} SCLK duty cycle		40	–	60	%
t_{CDS} CDATA setup time		25	–	–	ns
t_{CDH} CDATA hold time		25	–	–	ns
t_{RDS} RDATA setup time		25	–	–	ns
t_{RDH} RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1, 2 or more bytes of CDATA are sent to the peripheral MSB first, LSB (Bit 0) last. RDATA is read from the peripheral MSB first, LSB (Bit 0) last.
2. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
3. When reading from the 13 C-BUS registers listed in Table 3, the minimum time required before a C-BUS read operation ($t_{CSOFF(rd)}$) is 2000ns. For all other C-BUS read registers tCSOFF is a minimum of 50ns.

Table 3 Minimum tCSOFF for C-BUS Read

ADDR. (hex)	Read/ Write	C-BUS REGISTER	Word Size (bits)	Minimum tCSOFF before reading (ns)
$70	R	Internal Buffer Fill Level	16	2000
$71 to $74	R	AuxADC1-4 Read	16	2000
$75	R	I Offset	16	2000
$76	R	Q Offset	16	2000
$77	R	AGC Gain and RSSI	16	2000
$7A	R	Rx Error Magnitude	16	2000
$7B	R	Frequency Error	16	2000
$78	R	SPI Thru-Port Read	16	2000
$79	R	GPIO Input	16	2000
$7D	R	Programming Register Read	16	2000

9.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 50 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7364Q1

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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